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NASA CR-150213

(NASA-CR-150213) DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION Final Report, 30 Jun. 1969 - 14 Jul. 1976 (RCA Labs., Princeton, N. J.) 61 p HC A04/MF A01 CSCL 09C G3/33

N79-25317

Unclas 26856

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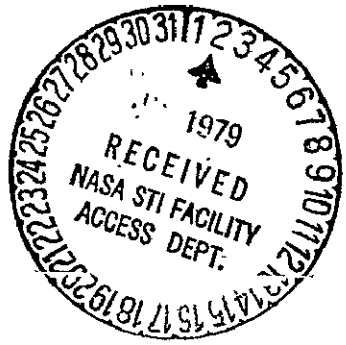
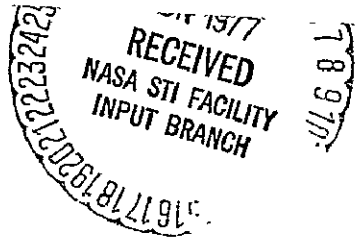
Princeton, New Jersey 08540

Final Report

August 1976





Prepared for

NASA - GEORGE C. MARSHALL SPACE FLIGHT CENTER
Marshall Space Flight Center, Alabama 35812

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA CR-150213		

4. Title and Subtitle	5. Report Date
DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION	August 1976
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
A. C. Ipri	PRRL-76-CR-42
9. Performing Organization Name and Address	10. Work Unit No.
RCA Laboratories Princeton, New Jersey 08540	
	11. Contract or Grant No.
	NAS12-2207
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Final Report (6-30-69 - 7-14-76)
George C. Marshall Space Flight Center National Aeronautics & Space Administration Huntsville, AL 35812	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

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17. Key Words (Selected by Author(s))

Large-scale integrated (LSI) ci
cuits
Silicon-gate fabrication
Integrated circuit technology

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	61	NTIS

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SUMMARY

This final report describes our progress in developing a method for determining the applicability of a particular process for the fabrication of large-scale integrated circuits. Test arrays were designed, built, and tested, and then they were utilized. A set of optimum dimensions for LSI arrays was generated. The arrays were also applied to yield improvement through process innovation, and additional applications were suggested in the areas of yield prediction, yield modeling, and process reliability.

I. INTRODUCTION

At present, large-scale integration (LSI) means the fabrication of semiconductor arrays containing several thousand devices in an area less than a quarter of an inch on a side with yield values in excess of 2%. These three factors, density, size, and yield, are, of course, all interrelated and depend, in turn, on two interdependent areas, process technology and physical dimensions (or design rules). It should be pointed out that this is not the case in small- or medium-scale integration where the degree of complexity is low and, hence, the yield is high and relatively independent of physical dimensions.

This program was concerned with large-scale integration, and, therefore, it was necessary to consider the impact of both the process technology and the physical dimensions on packing density, chip size, and array yield. In order to accomplish this it was necessary to perform an in-depth study of the particular process of interest, the silicon-gate deep-depletion CMOS/SOS process, to determine which steps or sequence of steps should be analyzed. It was also necessary to develop techniques for determining the interrelationships of various process sequences as well as the dimensional dependence of these sequences.

Once the process analysis was complete, the necessary test structures were designed and masks were generated. Three test structures were produced: the process analysis structure (PAS), the spacing array (SPAR), and the contact array (CAR). In addition, various processing sequences were developed to analyze the particular steps and sequence of steps of interest.

The test structures and procedures were then used to initiate a comprehensive program of process analysis and the design rule-process interaction. Yield data were generated for various critical process steps as well as the yield variation of the process step with physical dimensions. From these yield data it was possible to generate a set of curves relating the physical dimensions associated with a particular

process sequence to the expected number of working LSI arrays producible from these dimensions. In general the curves showed a peak value associated with a particular dimension indicating an "optimum" value. It was possible, therefore, to generate an optimum set of LSI design rules.

It was demonstrated that the various test structures were useful in evaluating new process techniques as well as new processing equipment, and yield data were generated comparing the old with the new. Also included in this report is an analysis of the various yield models which are being studied in the literature and their applicability to the data generated in this study.

II. PROCESS ANALYSIS AND EVALUATION STRUCTURES

Random defects can be generated by any of the various process steps used in the fabrication of integrated circuits. There are, however, certain specific steps of a critical nature which are used repeatedly and can be grouped together. These are:

(1) Thin-film deposition or growth
- Semiconductor layers
- Dielectric layers
- Metal layers

(2) Photoresist techniques

(3) Etching techniques

(4) Doping techniques

Nearly all integrated-circuit process technologies contain these categories. Different specific approaches, however, are used by different companies in each of these categories. Etching, for instance, may be the result of a wet chemical technique in one company while another may use a gaseous plasma approach. Ion implantation may be used as the doping source for some while others use high-temperature gaseous sources. The number of different photoresist techniques is endless. The need to examine these steps to determine the degree to which they have been successfully accomplished is extremely important and returns one to the problem at hand.

In general, a process sequence involves depositing, growing or doping a thin film, defining the film, and etching it. These three sequential steps comprise one block which can be interrogated for defects, and, if the number is found to be high, the film can be stripped and the steps repeated. Analyzing the CMOS/SOS silicon-gate process, one finds that the first sequence of steps is the deposition and patterning of the thin silicon film. The process analyis structures must,

therefore, be able to check for:

(1) Silicon island discontinuities

(2) Silicon island to silicon island short-circuits

The next step is the oxidation of the islands followed by the deposition of the polycrystalline silicon film. The polysilicon layer is then patterned, and, hence, the test structure must examine for:

(3) Polycrystalline silicon discontinuities

(4) Polycrystalline-silicon island short-circuits

(5) Polysilicon to polysilicon short-circuits

A layer of silicon dioxide is deposited, and contact holes are etched in the layer to permit the metal interconnect pattern to make electrical contact to the silicon islands and polysilicon gates. A test must be performed, therefore, to described.

(6) Contact hole open-circuits

The last layer which is deposited and defined is the metal interconnect pattern. The process analysis structure must, therefore, examine for:

(7) Metal discontinuities

(8) Metal to island short-circuits

(9) Metal to polysilicon short-circuits

(10) Metal to metal short-circuits

All of these data "must" be compiled on a statistical basis so that, for instance, the "probability" of opening a certain number of contacts can be ascertained. The test structures which can be used to analyze these problem areas as well as to determine their dependence on physical dimensions will now be described.

A. Process Analysis Structure (PAS)

The PAS test cell is shown in Fig. 1. Listed in Table 1 are the corresponding dimensions for each level.

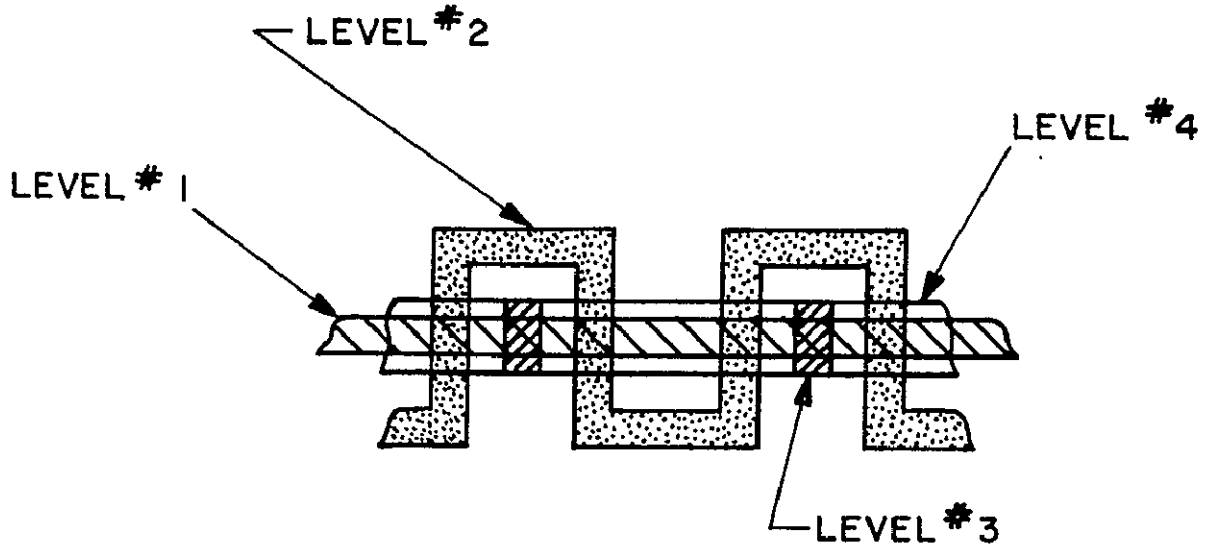

Figure 1. PAS test cell.

TABLE 1. PAS TEST CELL DIMENSIONS

Level No.	Length (mils)	Width (mils)
1	200, 400, 600, 1200, 2400, 4800, 7200	0.2
2	400, 800, 1200, 2400, 4800, 9600, 14400	0.2
3	0.4	0.2
4A	200, 400, 600, 1200, 2400, 4800, 7200	0.4
4B	200, 400, 600, 1200, 2400, 4800, 7200	0.3
4C	200, 400, 600, 1200, 2400, 4800, 7200	0.25
4D	200, 400, 600, 1200, 2400, 4800, 7200	0.20
4E	200, 400, 600, 1200, 2400, 4800, 7200	0.15
4F	200, 400, 600, 1200, 2400, 4800, 7200	0.10

A photomicrograph of a typically processed PAS is shown in Fig. 2. The basic concept inherent in this test structure is that the number of effective defects which are generated by a particular process step and are detrimental to the definition of a particular physical dimension can

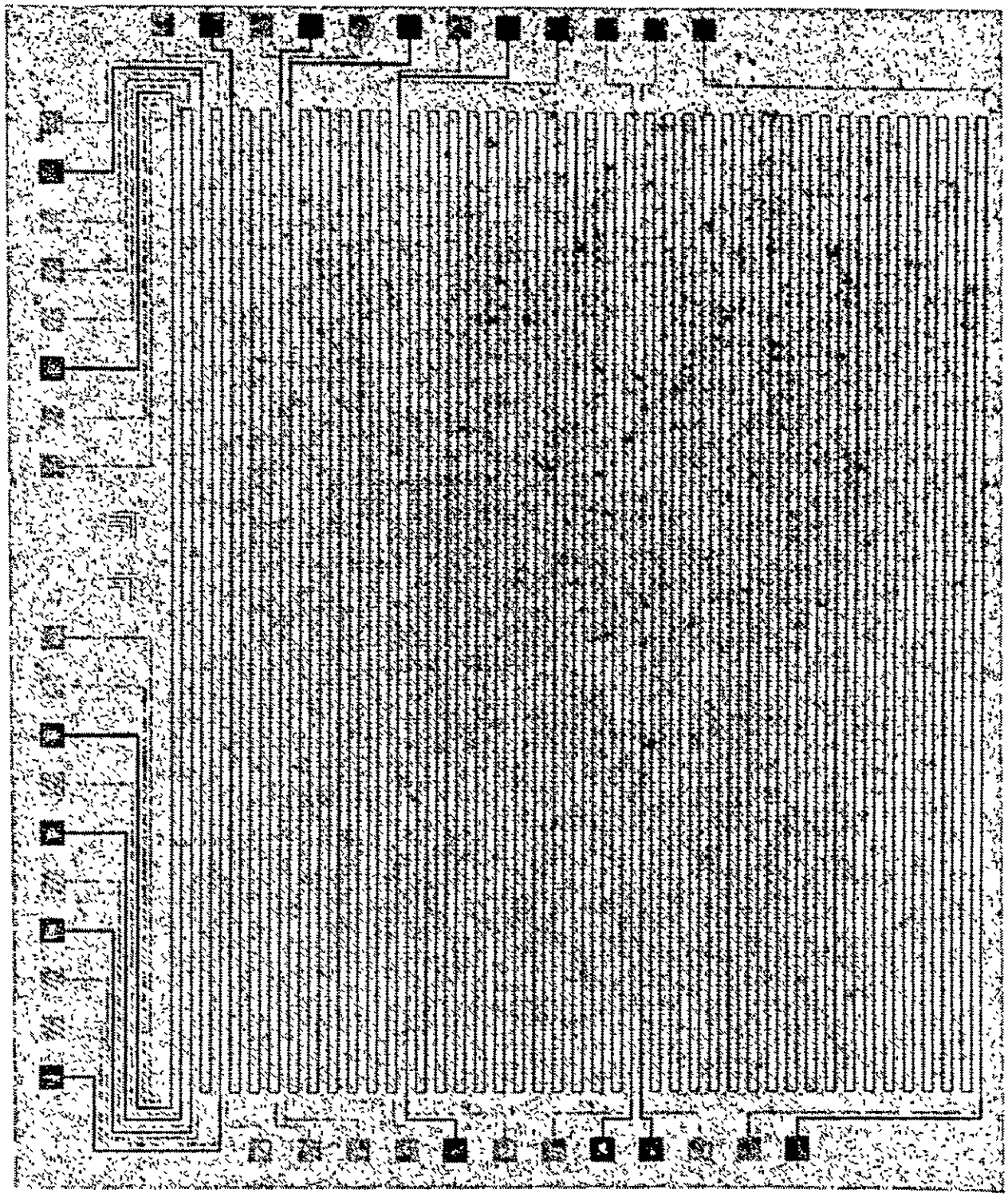

Figure 2. Photomicrograph of typically processed PAS.

be determined by "sequentially" interrogating the defined pattern. For this reason the array was laid out so that an increasing number of cells could be analyzed and a pass or fail condition determined as a function of the number of cells. The number of cells accessible for analysis and brought out to external pads were 200, 400, 600, 1200, 2400, 4800, 7200. The total array, therefore, contained 14,400 cells.

The levels listed in Table 1 can be used individually or in various combinations to determine the continuity of different types of conductors on the interaction of one layer with another. Some of the applications of this array will be discussed in the following sections.

B. Spacing Array (SPAR)

This array is concerned with the ability of a given process sequence to define conducting lines spaced a given distance apart. The SPAR cell is shown in Fig. 3 where it is seen that two masks levels can be used. The first level is used to define steps, if desired, over which the conducting lines are defined (level 2). The dimensions are given in Table 2.

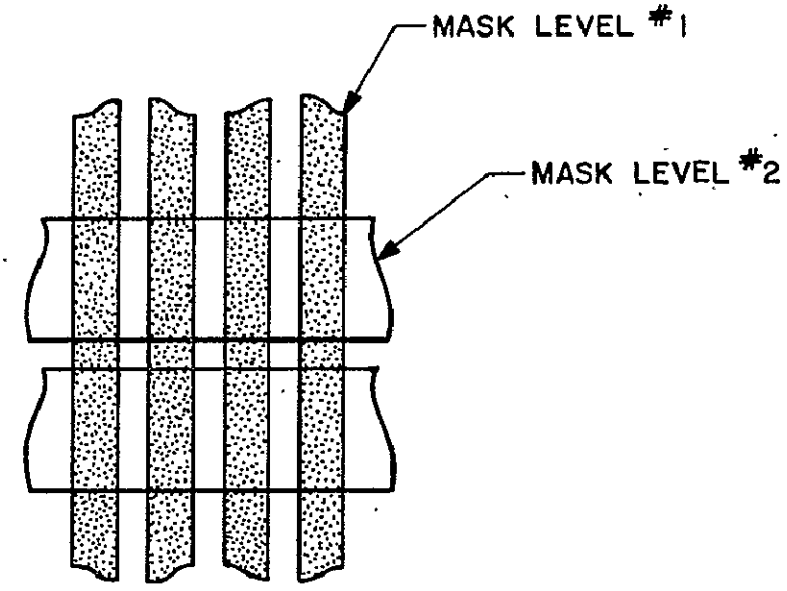

Figure 3. Line-to-line spacing array (SPAR).

TABLE 2. SPAR DIMENSIONS

Level No.	Width (mils)	Length (mils)	Separation (mils)
1	0.3	--------	0.20
2A	0.7	200, 400, 600, 1200, 2400, 4800, 9600	0.30
2B	0.75	200, 400, 600, 1200, 2400, 4800, 9600	0.25
2C	0.80	200, 400, 600, 1200, 2400, 4800, 9600	0.20
2D	0.85	200, 400, 600, 1200, 2400, 4800, 9600	0.15
2E	0.90	200, 400, 600, 1200, 2400, 4800, 9600	0.10

The width of the conducting lines was made greater than 0.7 mil in order to minimize the probability of discontinuities. A photomicrograph of level 2 is shown in Fig. 4.

C. Contact Array (CAR)

This mask set contains an array of SOS islands upon which contacts may be defined. The islands are then interconnected with metal, and the continuity of each contact string is interrogated. A cell of the CAR is shown in Fig. 5. The function and dimensions of each level are given in Table 3.

TABLE 3. CAR LEVEL FUNCTIONS AND DIMENSIONS

Level No.	Function	Dimensions (mils)
1	Islands	0.6 x 1.4
2	Polysilicon	0.2 x 1.0
3A	Contacts	0.3 x 0.4
3B	Contacts	0.3 x 0.3
3C	Contacts	0.25 x 0.25
3D	Contacts	0.20 x 0.40
3E	Contacts	0.20 x 0.30
3F	Contacts	0.20 x 0.25
3G	Contacts	0.20 x 0.20
3H	Contacts	0.20 x 0.15
3I	Contacts	0.20 x 0.10
4	Metal	0.7 x 1.4

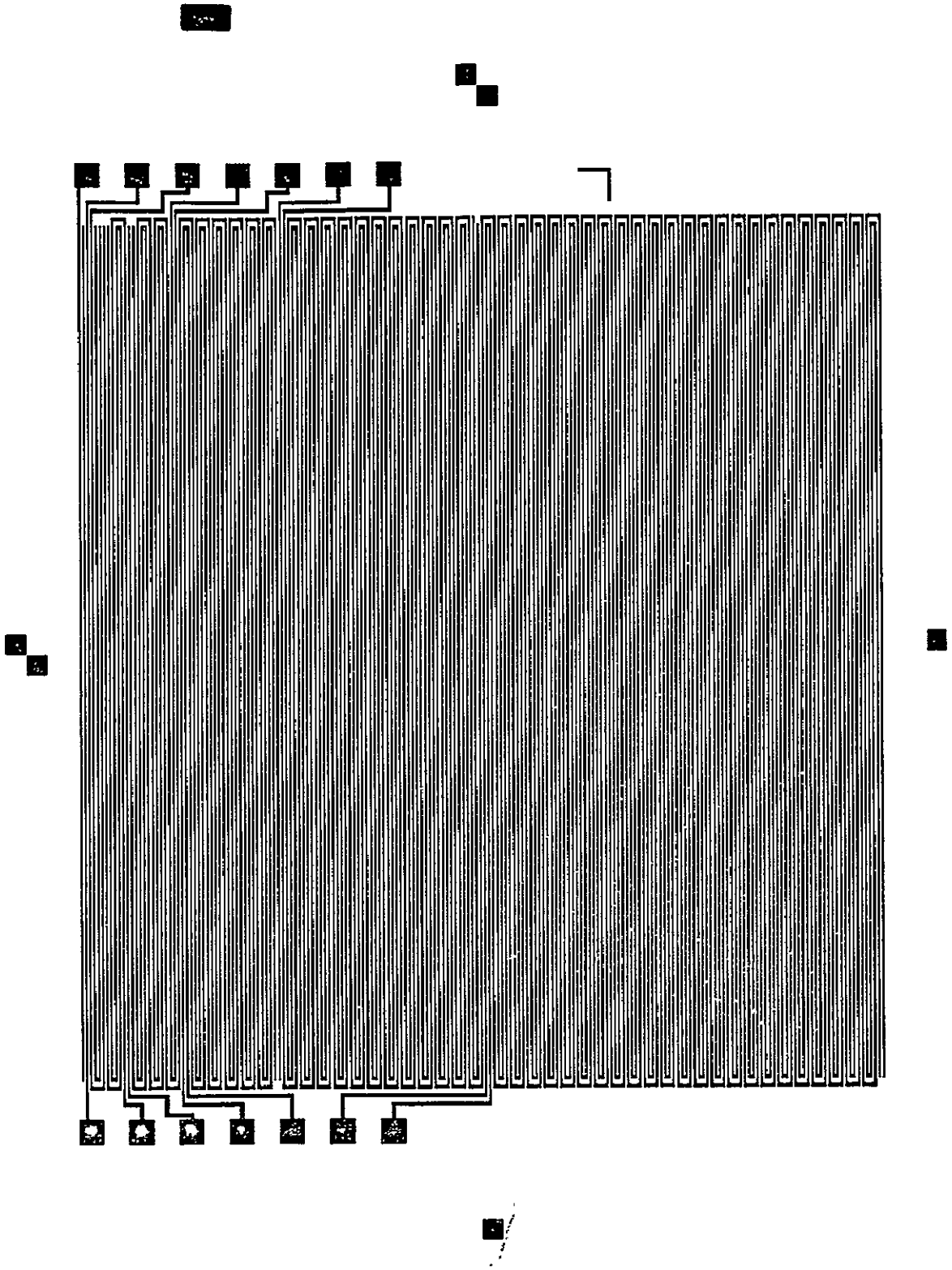

Figure 4. Photomicrograph of SPAR level 2.

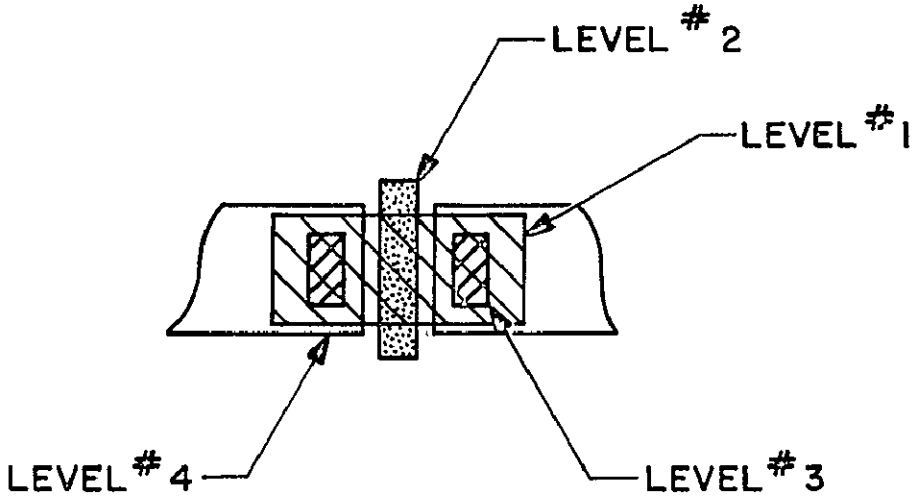

Figure 5. Contact array (CAR).

Level 2 can be used to define a material which allows control of the spacing between the contact mask and the photoresist which is to be patterned. The number of contacts which can be independently analyzed and are connected together to form a single string is listed below.

String No.	No. of Contacts
1	200
2	400
3	600
4	1200
5	2400
6	4800
7	9600
8	19200

A photomicrograph of the metal pattern is shown in Fig. 6.

These three test patterns can be used in a wide variety of applications in the areas of process analysis, integrity, and control as they relate to physical characteristics. They are obviously not intended to

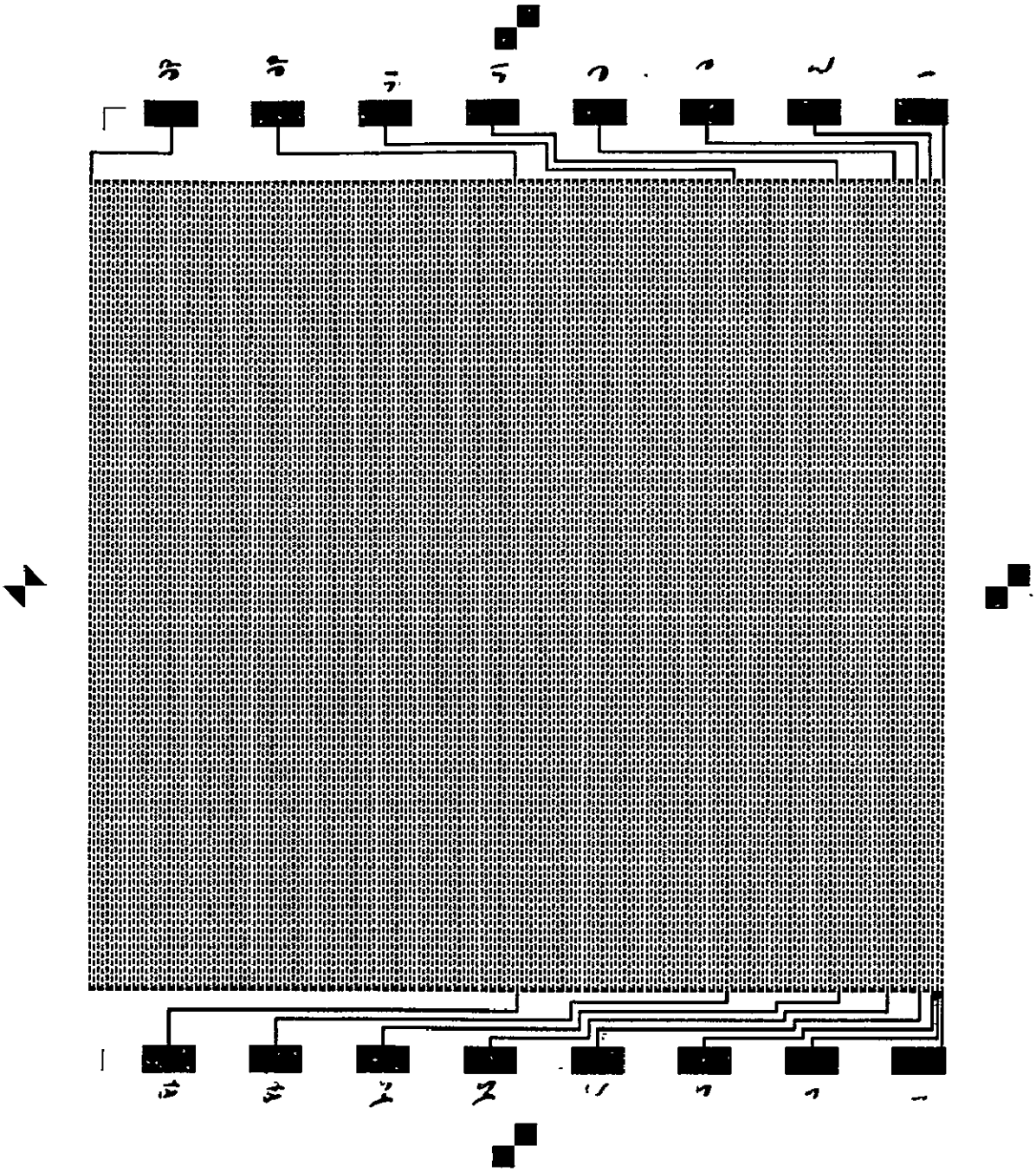

Figure 6. Photomicrograph of CAR metal pattern.

permit an in-depth analysis of transistor characteristics, but, as will be described in later sections, some interesting device-related electrical parameters can be obtained as they relate to physical dimensions and yield statistics.

III. CMOS/SOS PROCESS CHARACTERIZATION

The silicon-gate deep-depletion CMOS/SOS process has been described in the literature (ref. 1) and is shown diagramatically in Fig. 7. This process will now be discussed in detail to ascertain the process-dimension interaction as expressed in terms of yield curves, the object being to demonstrate the applicability of the various test arrays for process analysis and characterization.

A. Epitaxial Silicon Integrity

Various questions have been raised concerning the physical integrity of SOS films as well as the processing techniques which have been used to define them. Patterns were defined, therefore, using both the PAS and the SPAR masks to determine the yield associated with defining various lengths, widths, and spacings in single crystal silicon films on sapphire. The fabrication steps are listed below.

(1) Deposition of 0.6-μm silicon films on $(1\bar{1}02)$ sapphire (ref. 2)
(2) Thermal oxidation (900°C - HCl steam - 10 minutes)
(3) Photoresist (Waycoat 43 or GAF)
(4) Oxide etch (buffered HF)
(5) Silicon etch (KOH-n-propanol-H_2O) (ref. 3)
(6) Strip masking oxide (HF)
(7) Dope silicon pattern with boron ($1 \times 10^{20}/cm^3$)
(8) Electrically test

Various process techniques can be used to define the initial silicon pattern; our choice was a short thermal oxidation followed by the application of a positive resist (GAF). A 30-second etch in buffered HF which minimized undercutting defined the oxide pattern, and the silicon was patterned in an anisotropic KOH solution (ref. 3).

Mask levels 4B through 4F of the PAS were used to determine the integrity of epitaxial silicon lines while levels 2A through 2E of the

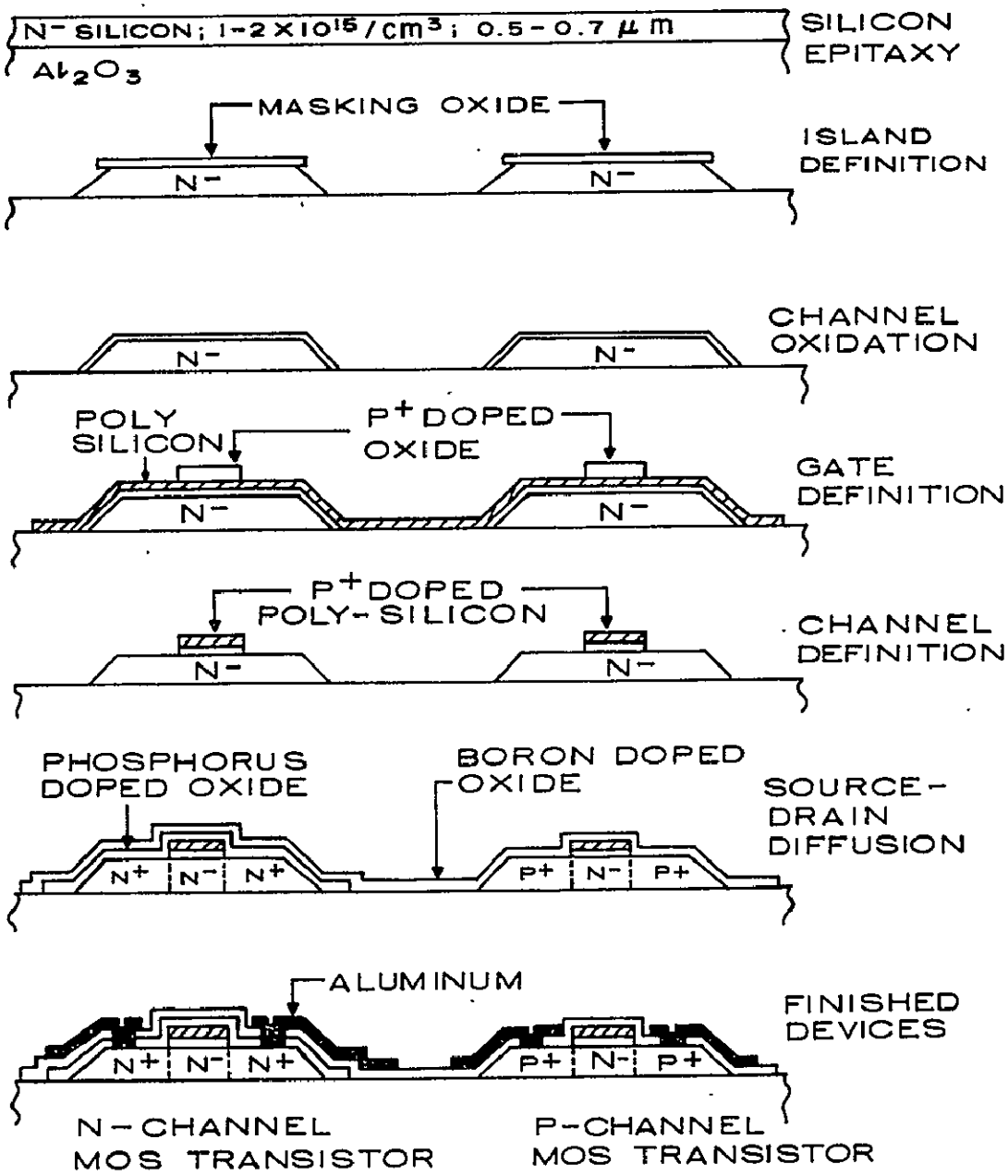

Figure 7. Silicon-gate deep-depletion CMOS/SOS process.

SPAR permitted the evaluation of epi-to-epi spacings. The results are shown in Fig. 8. The numbers in parentheses are the nominal mask dimensions while the other number is the dimension actually printed in the silicon (+0.020 mil). The present SOS design rules within RCA call for 0.20-mil minimum epi-silicon width and spacing, and it is seen from Fig. 8 that this value is certainly sufficient to permit the fabrication of high yield arrays. It is interesting to note that:

(1) Even the loosest dimensions (i.e., 0.3-mil width and 0.3-mil spacing) do not result in a length-independent yield value out to 12 inches (Y > 0.9).

(2) The yield values for the dimensions studied were relatively tightly clustered (i.e., slight variations with width).

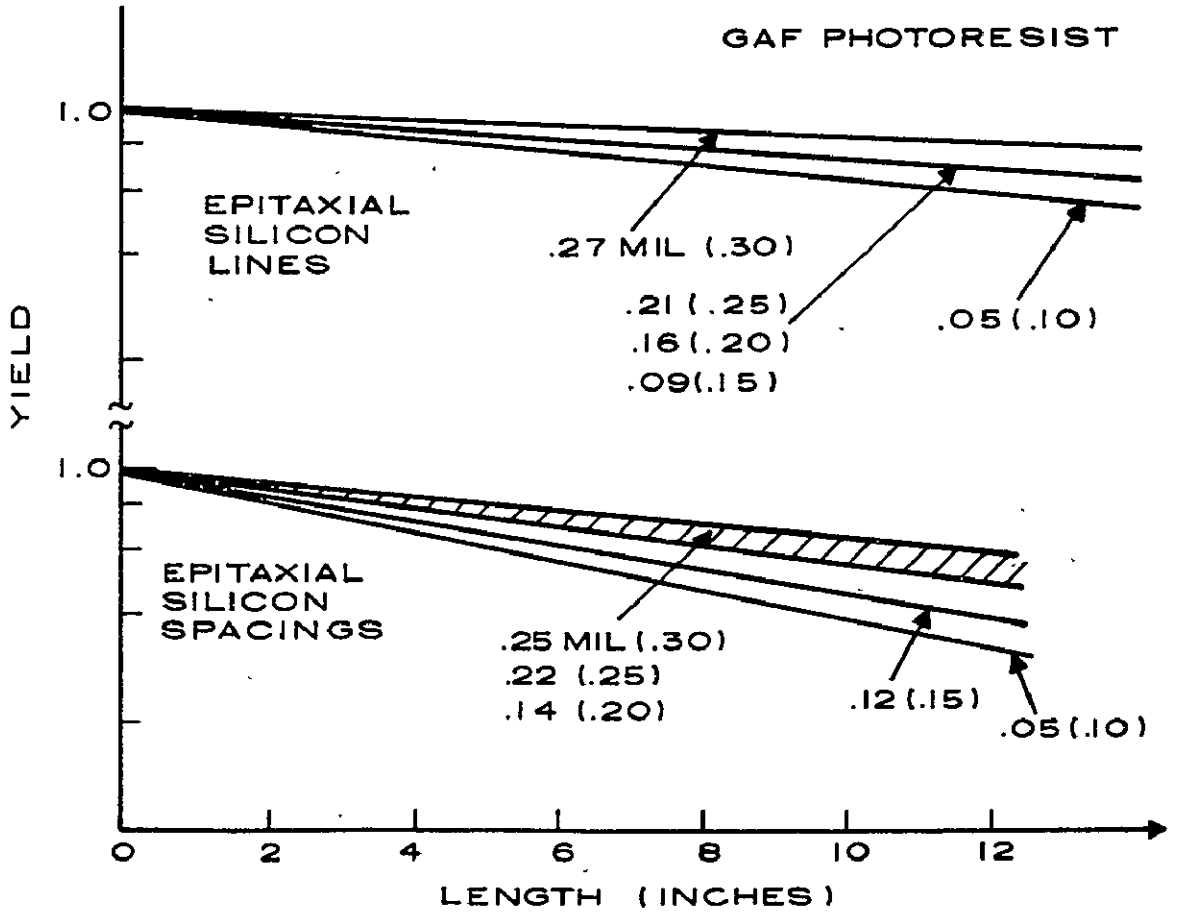

Figure 8. Yield as a function of length, epi-silicon.

It will be shown later that this situation is not always the case. It was initially thought that mask defects were the cause for yield reduction with loose dimensions. Later results with aluminum metallization, however, show that this was not so. The results, therefore, appear to indicate that (1) the silicon films contain defects which are rather large in size and (2) the density of smaller defects does not appear to increase rapidly as the size of the defect (or dimension) is reduced. In addition, the fabrication of arrays with epitaxial silicon dimensions of 1 to 2 μm appear to be within the present process technology.

B. Polycrystalline Silicon Technology

After the epitaxial silicon has been defined, the channel oxide is grown, polycrystalline silicon is deposited, and defined. Before examining the interaction of the polycrystalline silicon with the epitaxial silicon, the integrity of the polysilicon was examined without the presence of the epi-layer. The process sequence was:

(1) Chemically vapor deposited silicon from SiH_4 in H_2 at 700°C (5000 Å).
(2) Deposition of boron-doped SiO_2 (1000 Å)
(3) Deposition of undoped SiO_2 (1000 Å)
(4) Photoresist (Waycoat)
(5) Etch oxides (buffered HF)
(6) Diffusion (1050°C - 15 minutes - He)
(7) Strip glass (buffered HF)
(8) Etch polysilicon (KOH-n-propanol-H_2O)
(9) Test wafers

This is a P+ polysilicon process incorporating P+ doped SiO_2 as the diffusion source. The disadvantage of this process is that the pattern must be defined in the two SiO_2 layers before being transferred to the polycrystalline silicon. The advantage, however, is that the P+ doped silicon is unetchable in KOH, and, hence, the etching process is a

self-limiting one. Again, as with the epi-silicon layer, the PAS and SPAR masks were used to define various lengths, widths, and spacings. The integrity of the various polycrystalline silicon patterns is shown in Fig. 9. In general, the results show that:

(1) Large area defects do not appear to be present.

(2) A substantial increase in defect density with decreasing defect size (or physical dimension).

(3) Process techniques for defining fine line geometries produce a lower yield on polycrystalline silicon then on epitaxial silicon.

As is evident in Fig. 9 the defects are width-limiting rather than spacing-limiting. In addition, the relatively wide lines and spacing show little yield dependence on length over the region investigated. The present design rules limit the polysilicon width and spacing to 0.2 mil which, as shown in Fig. 9, are high yield dimensions.

C. Epitaxial Silicon-Polycrystalline Silicon Interaction

The integrity of defining polycrystalline silicon over epitaxial steps is, of course, the real world and several of these investigations remain to be carried out. Using the PAS, however, tests have been carried out where mask level 1 was used to define single crystal islands using the process defined in Section III.A. After the integrity of these patterns was determined, the islands were oxidized (900°C - HCl steam - 45 minutes) and the polysilicon process was applied using mask level 2. It was possible, therefore, to determine the continuity of 0.2-mil polycrystalline silicon lines as a function of length. These data are given in Fig. 10. Comparing Fig. 10 with Fig. 9 shows that for 0.2-mil polysilicon lines, there is no measurable yield reduction due to the nonplanarity of the polysilicon layer. It is felt, however, that this will not be the case for narrower widths.

Once the integrity of the epitaxial and polycrystalline silicon lines had been ascertained, it was possible to examine the integrity of

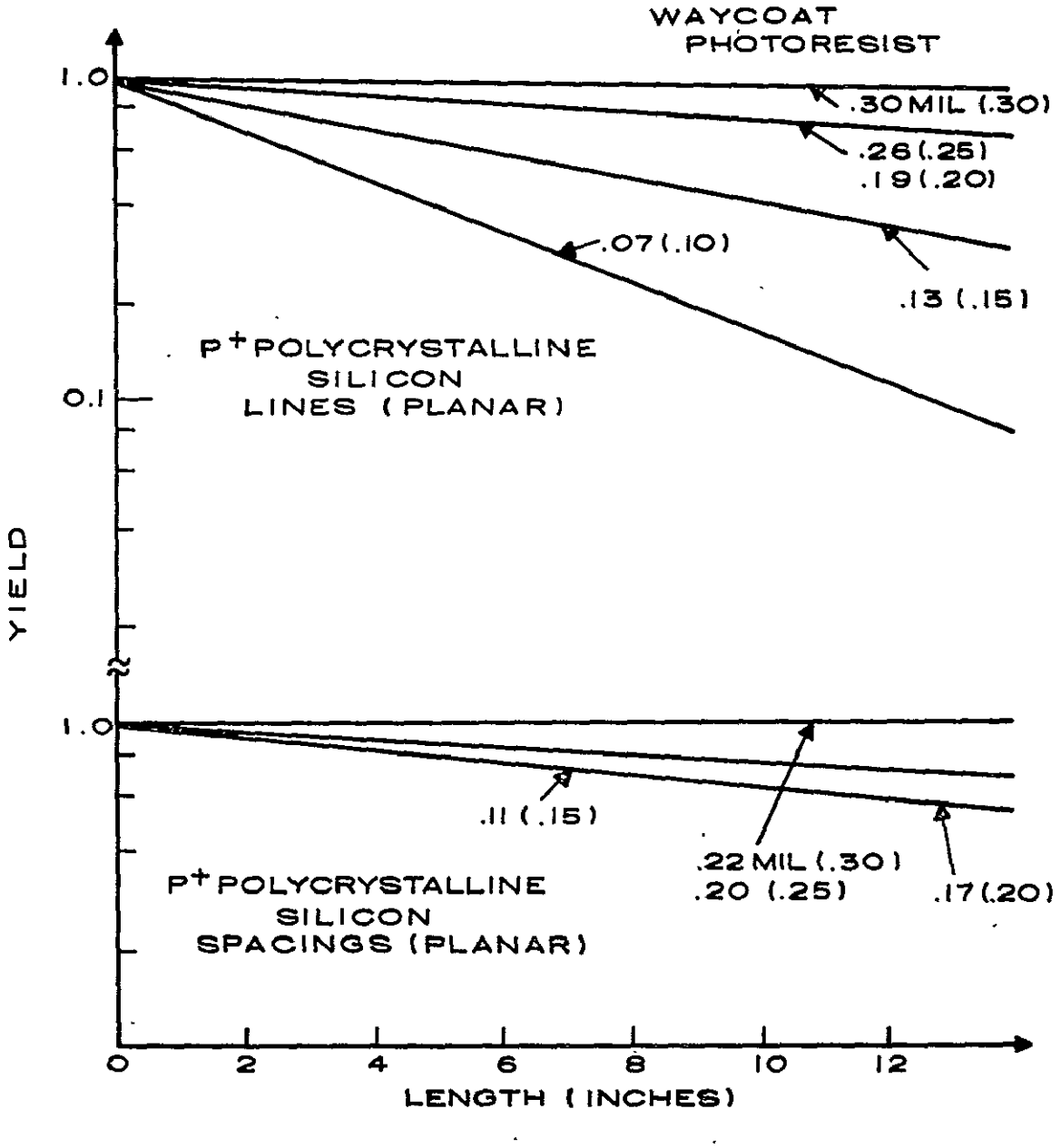

Figure 9. Yield as a function of length, polycrystalline silicon.

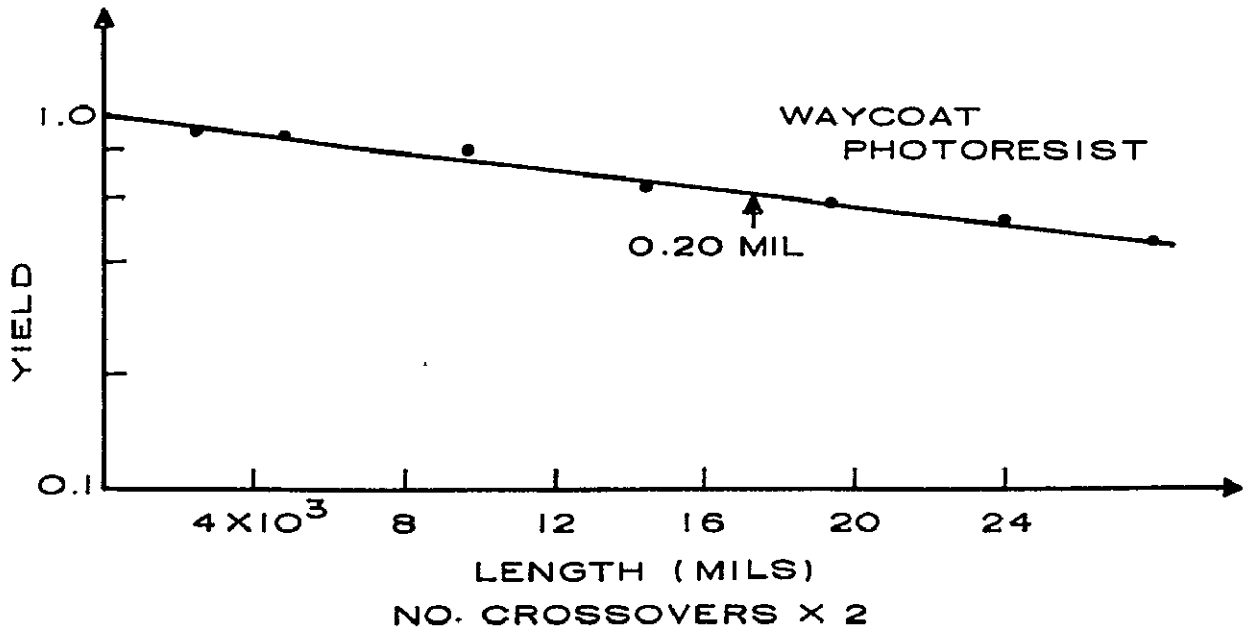

Figure 10. Yield as a function of length, polycrystalline silicon crossing over epi-silicon.

the channel oxide. Since the epitaxial layer was doped prior to oxidation, it was possible to test for polysilicon to island short-circuits both before and after the self-align etch of the channel oxide which removes it from the sources and drains of the devices. It has been found that the integrity of the channel oxide as determined by the number of short-circuits which are present between the epitaxial silicon island and the P+ doped polysilicon gate is extremely variable. This is demonstrated in Fig. 11. It has been shown previously (ref. 4) that the dielectric strength of the channel oxide on the edge of a silicon island is poor but can be improved in any of several ways. In Fig. 11, case 1 is a standard channel oxide which has been grown in HCl steam at 900°C for 45 minutes. Case 2 was oxidized in the same manner followed by the deposition of 500 Å of SiO_2. The resulting dielectric strength increased substantially and, as shown in Fig. 11, the yield was also substantially improved. Other techniques such as depositing Si_3N_4 in place of the SiO_2 or replacing the deposited SiO_2 with oxidized polycrystalline silicon have also shown similiar results.

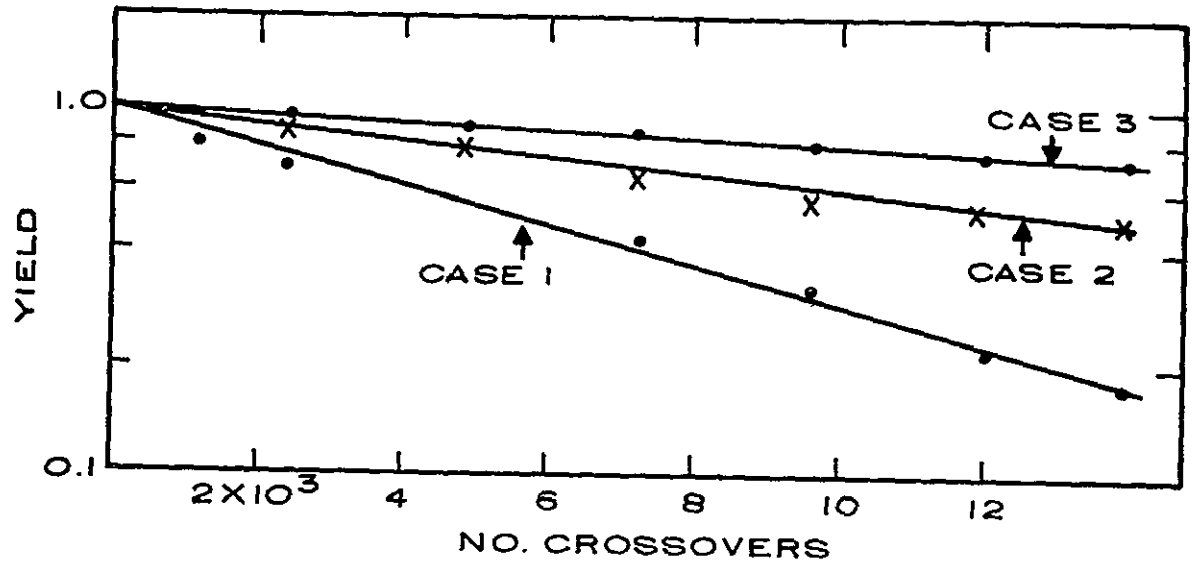

Figure 11. Channel oxide integrity; yield as a function of the number of crossovers.

It has been shown, therefore, that both the dielectric strength of of SOS/MOS devices as well as the yield associated with LSI arrays can be substantially improved with the addition of the proper process modification. In addition to the edge-related yield-reducing mechanism, there is another problem area associated with the self-align etch of the channel oxide. The yield, therefore, can be further increased if the channel oxide is not removed. Case 3 demonstrates the improved integrity of the channel oxide which has not been removed from the source-drain areas. In order to fabricate devices with this technique it is necessary to incorporate ion-implantation to achieve source-drain doping. It should be noted that the channel oxide integrity varies widely from run to run, and hence the data presented here indicate typical results. Further study is needed in this area in order to achieve consistently high oxide integrity.

D. Contact Integrity

Initial runs have been completed using the CAR masks. Attempts were made to print and etch levels 3C, 3F, 3G, 3H, and 3I on thermally oxidized silicon islands as well as islands covered by deposited oxides. A negative photoresist (Waycoat 43) was used for pattern definition, and, in general, it was found that the printed contact opening had each dimension reduced by approximately 0.05 mil when compared with the mask dimension. Using the usual control techniques, the pattern, as defined in the photoresist, could be replicated in the oxide to a high degree of precision. Some typical results are shown in Fig. 12. It is seen that mask dimensions larger than 0.25 x 0.25 mil should have been investigated in order to observe a high yield (Y > 0.9) curve. In addition, there appears to be a rapid reduction in yield for contact openings less than 0.16 x 0.16 mil.

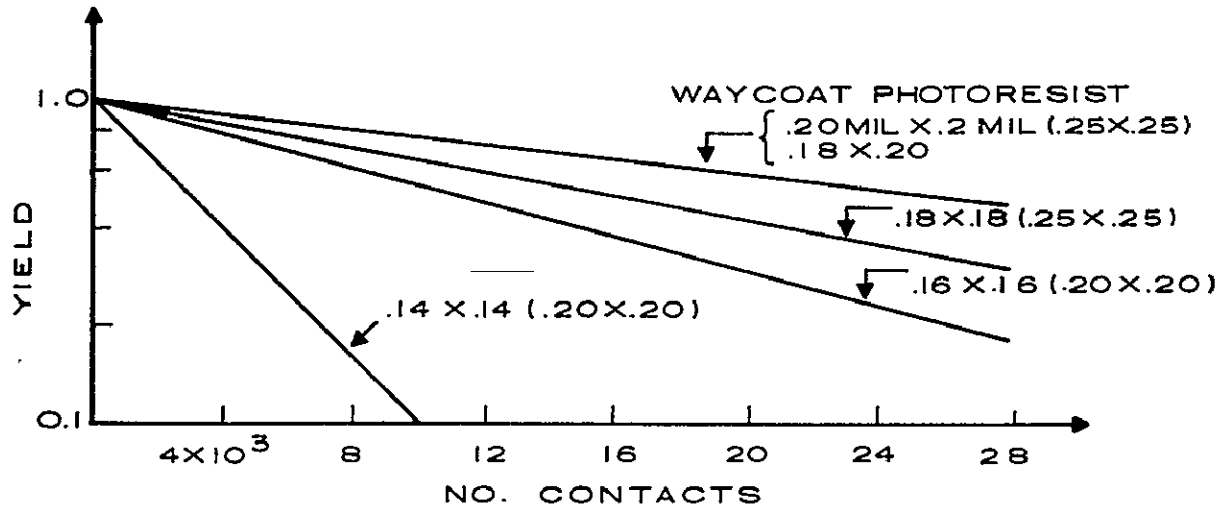

Figure 12. Contact integrity; yield as a function of the number of contacts.

Further experiments need to be conducted using mask level 2 which separates it from the photoresist area to be exposed. The use of rectangular contacts should also be studied. Initial results seem to

indicate that for a given contact area, the resulting yield is higher for rectangular than square contacts.

E. Interconnect Metal Integrity

As described in Section II, there are several aspects of the metallization step which must be analyzed. The initial discussion will be concerned with metal discontinuities followed by metal-to-metal short-circuits and, lastly, metal crossover short-circuits.

Concerning metal continuity, 1.4 μm of aluminum was evaporated, in an ion-pumped evaporation with a Sloan planetary system and electron-beam source, onto various surfaces. Both Shipley 1350 and Waycoat 43 were used in conjunction with PAS mask levels 4A through 4F to define various metal widths and lengths. The pattern was transferred to the aluminum using the standard, commercially available aluminum etch. The types of surfaces considered were:

- Planar (bare sapphire)
- Epitaxial silicon steps (0.6 μm)
- Polycrystalline silicon steps (0.5 μm)
- Multiple doped oxide steps (0.72 μm)

Mask level 2 was used to define the initial step pattern in the various materials. Typical results for Waycoat 43 photoresist are shown in Fig. 13. As expected the best results were obtained from the planar surface. This was the only surface which had continuous lines (although low yield ones) in the 2-μm width range. Results obtained on surfaces containing epi-silicon steps or polysilicon steps were approximately the same.

For the case where steps were etched in multiple doped deposited oxides, the lowest continuity yields were measured. These steps were fabricated by first depositing 800 Å of N+ doped oxide ($\sim 10^{20}/cm^3$) followed by 800 Å of undoped oxide. Next, 800 Å of P+ doped oxide

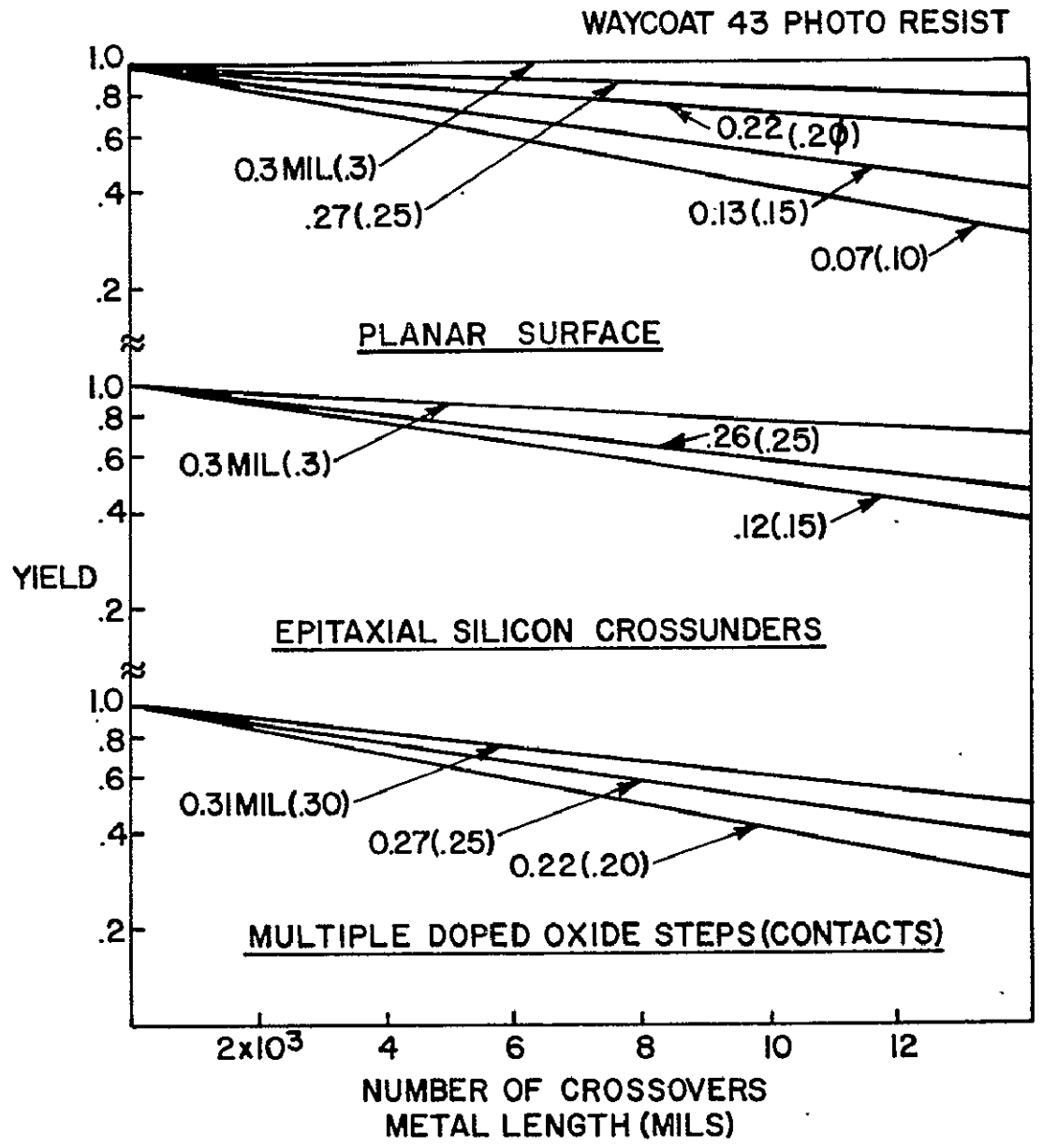

Figure 13. Interconnect metal integrity using CAR; yield as a function of the number of crossovers.

($\approx 10^{20}/cm^3$) were deposited followed by 4000 Å of undoped oxide. These layers were then densified at 1050°C in He for 15 minutes. As shown in Fig. 7, this closely duplicates the source-drain doping schedule. Defining mask level 2 of the PAS, therefore, is analogous to opening

contacts through these oxide layers. The continuity of metal lines which run over these doped oxide steps is a measure of the integrity of metal which must make contact to silicon through an opening which is "wider" than the metal line. In various SOS/LSI arrays metal lines make contact with several silicon islands through contact openings which may be wider than the width of the metal, and, hence, its integrity must be quantitively determined. It should be noted that this measurement is different from that which is conducted using the CAR. The contact array (CAR) interrogates the contact opening only; the metal interconnect is extremely wide (0.7 mil) and covers the contact opening on all four sides; hence, the probability of metal continuity into the opening is essentially unity. In review, therefore, best results were obtained on planar surfaces, with epi and poly steps causing measurable yield reductions and multiple doped deposited oxides producing the worst yield figures.

Aluminum patterns were defined using the SPAR masks, and, again, data were generated with and without steps. The results are shown in Fig. 14. As in the case for metal widths, best results (i.e., highest yields) were obtained on planar surfaces. It is interesting to note that even on a planar surface it was not possible to etch a spacing of 0.10 mil even though the photoresist definition looked extremely good. This is consistent with the general conclusion that pattern definition in aluminum produces substantially lower yield values for width and spacing than pattern definition in polycrystalline silicon which, in turn, produces lower yield values than pattern definition in single-crystal silicon.

Similar data were generated using Shipley 1350J photoresist and it was found that, for our photoresist procedure, substantial undercutting of the resist occurred during etching, producing at least a 0.1-mil reduction in metal widths or increase in metal-to-metal spacings.

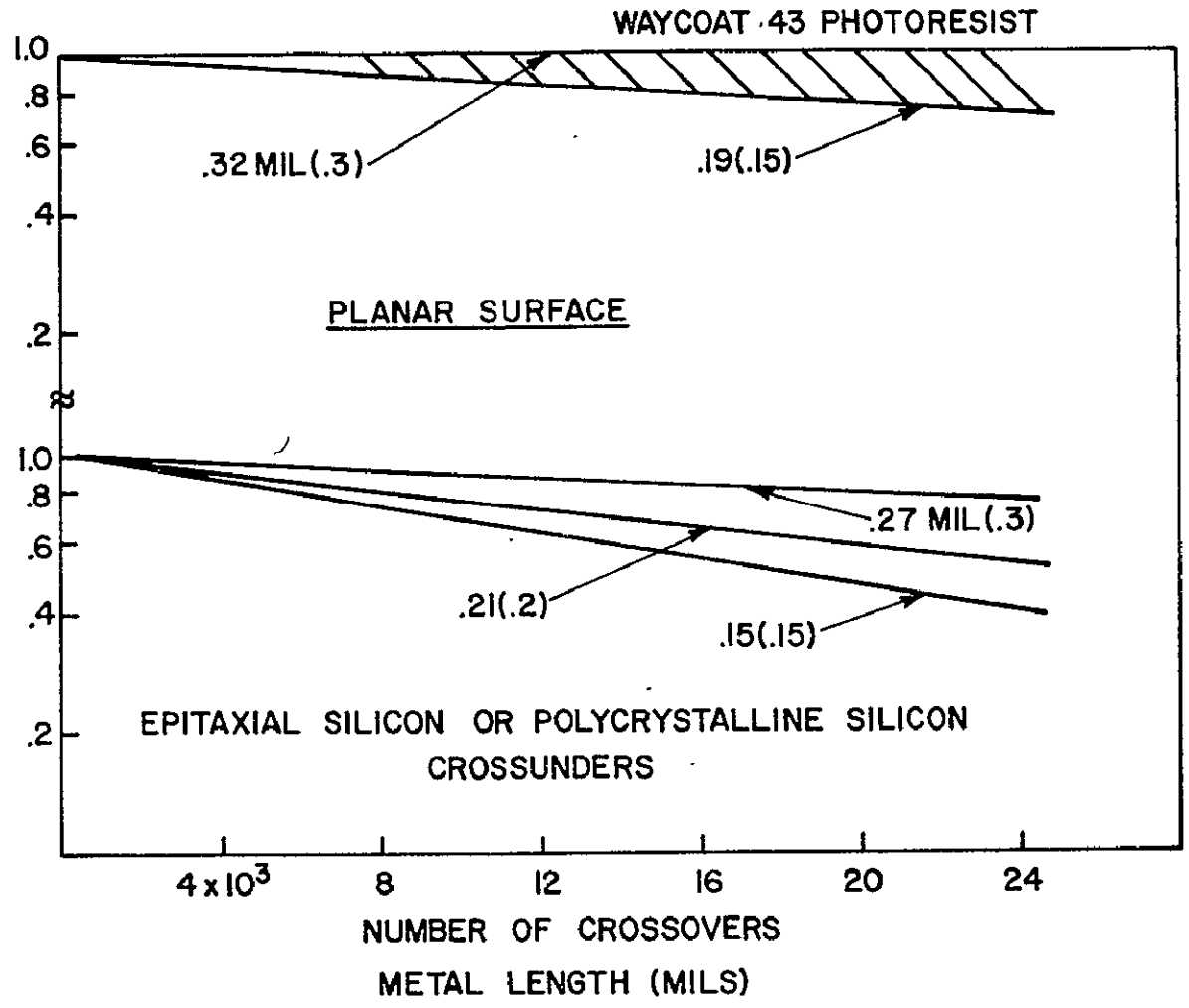

Figure 14. Interconnect metal integrity using SPAR; yield as a function of the number of crossovers. (Waycoat 43 photoresist).

Figure 15 shows typical results using Shipley. It is interesting to note, however, that for a given printed metal width, the yield values were higher for Shipley (positive) than Waycoat (negative). The use of Shipley for fine line geometries, however, is questionable because of the severe undercutting which results.

The final area of interest in the integrity of the field oxide which separates the metal conductors from polycrystalline or epitaxial silicon crossunders. This field oxide is again the multiple doped

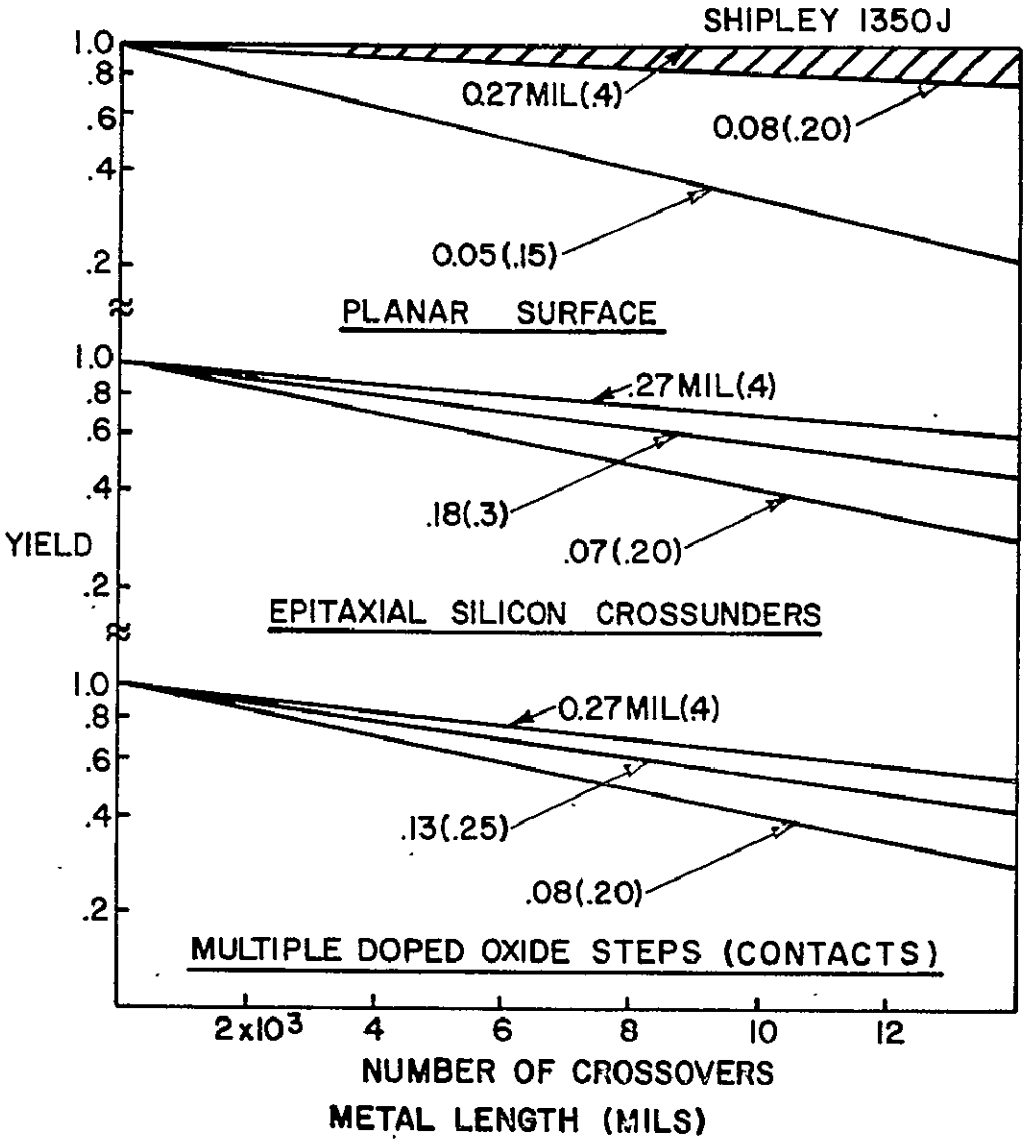

Figure 15. Interconnect metal integrity using SPAR; yield as a function of the number of crossovers (Shipley 1350J photoresist).

oxide which has been described in detail previously. Mask level 2 of the PAS was used to define the crossunders followed by the deposition of the doped oxides. Mask level 4B delineated the metal lines, and measurements were performed to determine the number of metal-to-cross-under short-circuits. The yields in general were in the 90% vicinity.

Worst-case results were obtained using mask level 1 to define single-crystal silicon lines. These were then oxidized and doped following the procedure in Section III.A; polycrystalline silicon was then deposited and defined using mask 2 and the procedure outlined in Section III.B; the field oxide was deposited; and the metal pattern was defined using mask level 4B. The number of short-circuits between the various sublayers was determined and the results are shown in Fig. 16. This is analogous to running metal conductors over the gates of SOS/MOS transistors. It is seen from Fig. 16, however, that the integrity of the field oxide, even under these conditions is extremely good and does not represent a substantial yield-limiting factor.

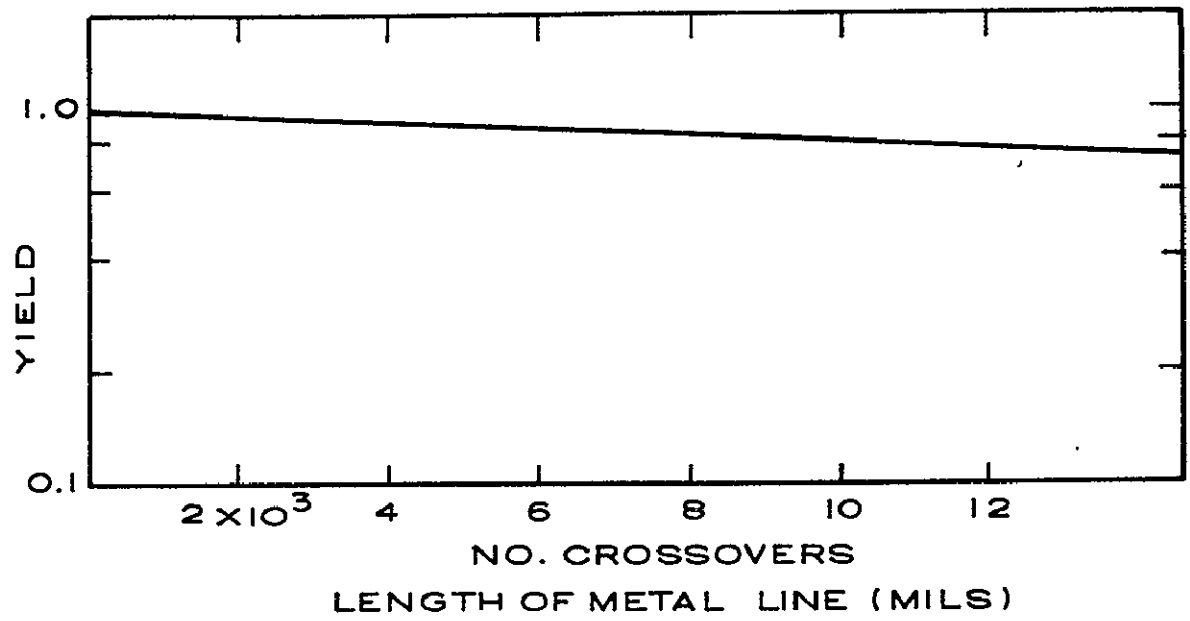

Figure 16. Field oxide integrity; yield as a function of number of crossovers.

F. SUMMARY

The three test arrays described in Section II have been used to analyze a particular process, namely, the silicon-gate deep-depletion CMOS/SOS process. From the data generated to date, three problem areas

have been uncovered and warrant future investigation. The first, which is strictly process related, concerns the integrity of the channel oxide. The yield curves showing the number of gate to island short-circuits have been widely variable and, for LSI arrays, can dominate the final yield.

The second area is process-dimension related and involves the non-planar nature of the present process. As can be seen from the yield curves, a substantial yield reduction is incurred due to steps. Our ability to pattern various layers (epi-silicon, polysilicon, aluminum) on a planar surface is substantially better than it is on a nonplanar surface.

The third area is also process-dimension related and is concerned with contact openings. At present, fine line patterns can be defined (at least on a planar surface) with decent yield, but the size of the contact which must be used to connect one layer to another must be larger than either level, to have a relatively high probability of opening. The physical dimensions of the array and, hence, the packing density, become dominated by the size of the contact opening.

All of these problem areas are essentially yield related. With the advent of new process techniques, yield values, as related to a fixed set of dimensions, will increase, and for a given set of yield values, it will be possible to reduce dimensions and, correspondingly, increase packing density.

IV. DESIGN RULE OPTIMIZATION

The previous section related process technology to physical dimensions through the generation of yield curves. In general, as physical dimensions are reduced, the corresponding yield associated with producing that dimension is also reduced. But, as these dimensions are reduced, the packing density, or number of chips per wafer, is increased. An extremely important parameter, therefore, is the number of "functioning" chips per wafer, which is dependent upon both the yield and packing density. Consider the expression:

$$\text{number of chips/wafer} = \frac{\text{wafer area}}{\text{chip area}} \tag{1}$$

and

$$\text{number of good chips/wafer} = \frac{\text{yield x wafer area}}{\text{chip area}} \tag{2}$$

The chip area is, of course, proportional to the various physical dimensions used to lay out the array. There are three cases of interest: (1) Both the length and width of the array may be functions of a particular physical dimension (or design rule); this will be referred to as the two-dimensional design limitation. (2) Either the length or the width alone may vary with a particular design rule; this is the case of one-dimensional design limitation. Lastly, the array area may not be a function of the particular design rule being considered.

For the case of two-dimensional design limitations, Eq. (2) becomes:

$$\text{number of good chips/wafer (2D)} = a\ \frac{\text{yield}_d}{(\text{dimension})^2} \tag{3}$$

where a is the constant of proportionality. In the one-dimensional case:

$$\text{number good chips/wafer (1D)} = b\ \frac{\text{yield}_d}{(\text{dimension})} \tag{4}$$

and, of course, for the third case,

$$\text{number of good chips/wafer} = C\ (\text{yield}_d) \tag{5}$$

and, hence, is simply a function of yield (i.e., the looser, the better). In some applications it is convenient to consider the width of a particular line as well as the spacing between the particular lines, and, hence, Eqs. (3), (4), and (5) become:

$$\text{relative number of good chips/wafer (2D)} = \frac{Y_w \times Y_s}{(w + s)^2} \tag{6}$$

where Y_w is the yield associated with a particular line width, Y_s is the yield associated with a particular line-to-line spacing, w is the line width, and s is the line-to-line spacing. Correspondingly,

$$\text{relative number of good chips/wafer (1D)} = \frac{Y_s \times Y_w}{(w + s)} \tag{7}$$

and

$$\text{relative number of good chips/wafer} = Y_s \times Y_w \tag{8}$$

The yield data as given in Section III will now be inserted into the suitable expressions, and curves relating the relative number of good chips per wafer to the specific physical dimensions will be generated.

A. Epitaxial Silicon on Sapphire Films

Using the data from Fig. 8 and Eqs. (6) and (7), the curves relating the relative number of good chips per wafer to the epitaxial silicon width and spacing are given in Fig. 17. It is interesting to note that neither curve in Fig. 17 exhibits a peak value. This is directly related to the relatively small variation in yield with epi-silicon widths or spacings. As will be seen later, this is not typical.

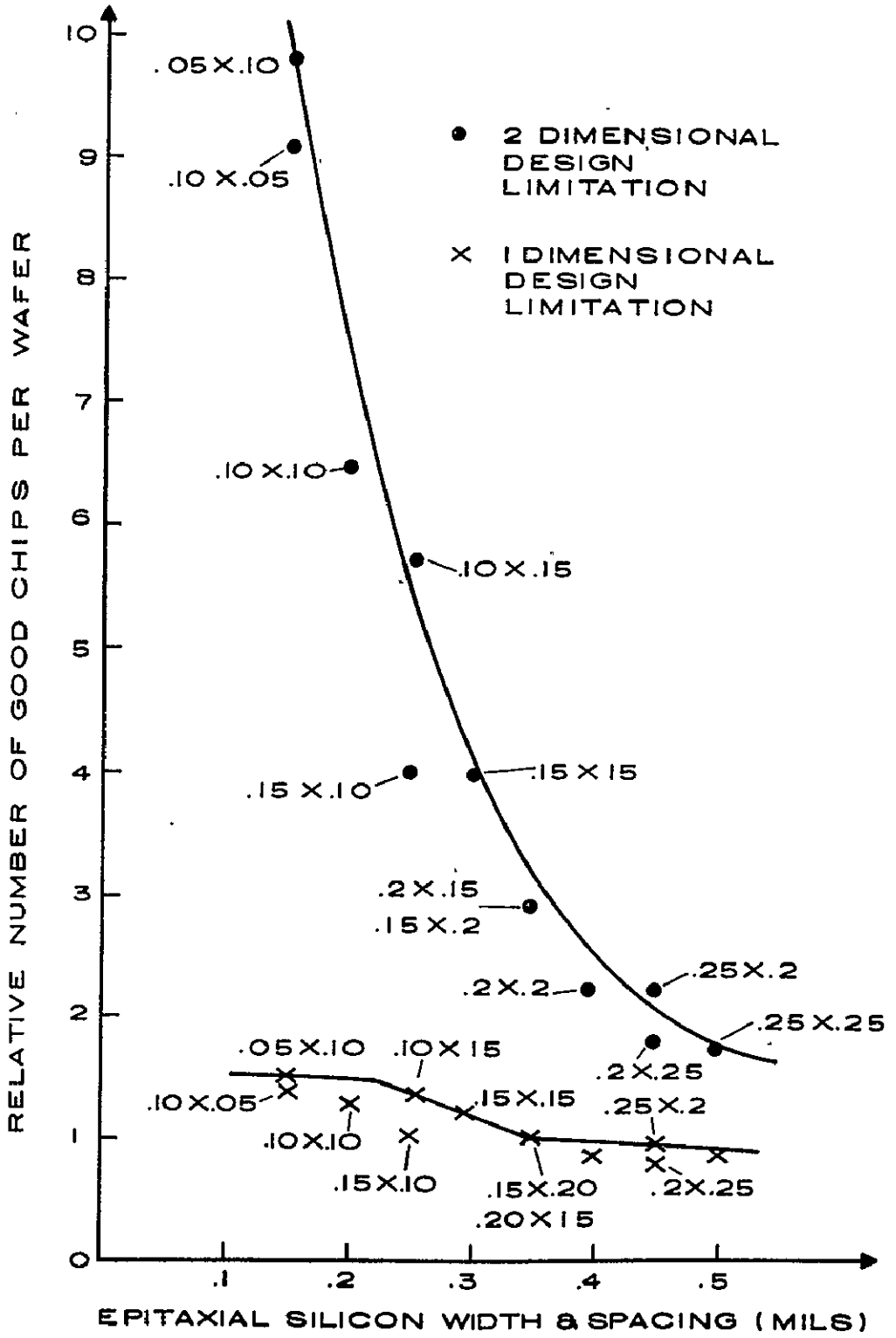

Figure 17. Good chips per wafer as a function of width and spacing, epi-silicon.

It also indicates that mask dimensions smaller than 0.1 mil are necessary to find optimum values for these particular parameters. The figure also shows substantial increases in the relative number of good chips obtainable per wafer for the case where both the length and width of the array are a function of the epi-width and spacing. This is not the case for the one-dimensional situation where the increase in packing density is almost balanced by the corresponding decrease in yield.

From the data presently available, it appears that the use of 0.1-mil epitaxial silicon lines separated by 0.1 mil is close to optimum values. A variation in either parameter of ±0.05 mil will not substantially reduce the yield of an array fabricated with these dimensions. It should be noted that these are "actual printed dimensions," and care must be taken when selecting mask or layout dimensions that the process will produce these dimensions as the end result.

B. Polycrystalline Silicon Layers

For the case of planar polysilicon lines and spacings, there is sufficient data from Fig. 9 to generate a similiar set of curves to that obtained for epi-silicon. Figure 18 shows the results of applying Eqs. (7) and (8) to the data from Fig. 9. The non-dimensional case, of course, simply reflects the yield variation which, as shown in Fig. 9, tends to saturate at a value of 0.3 mil. For the one-dimensional case, it is seen that widths and spacings in the 0.2- to 0.3-mil range tend to flatten, indicating an optimum value of about 0.25 mil for P+ polysilicon widths and spacings. The two-dimensional case, using Eq. (6), is shown in Fig. 19, and a peak is observed at a polysilicon width of 0.2 mil and a spacing of 0.15 mil. As shown in Fig. 9, the dimensional control using the process described in Section III.B is quite good, and the 0.2-mil width and 0.15-mil spacing should be reproducible from mask to defined poly-line. Again, it should be pointed out that the numbers in Figs. 18 and 19 are actual printed dimensions in the P+ polysilicon.

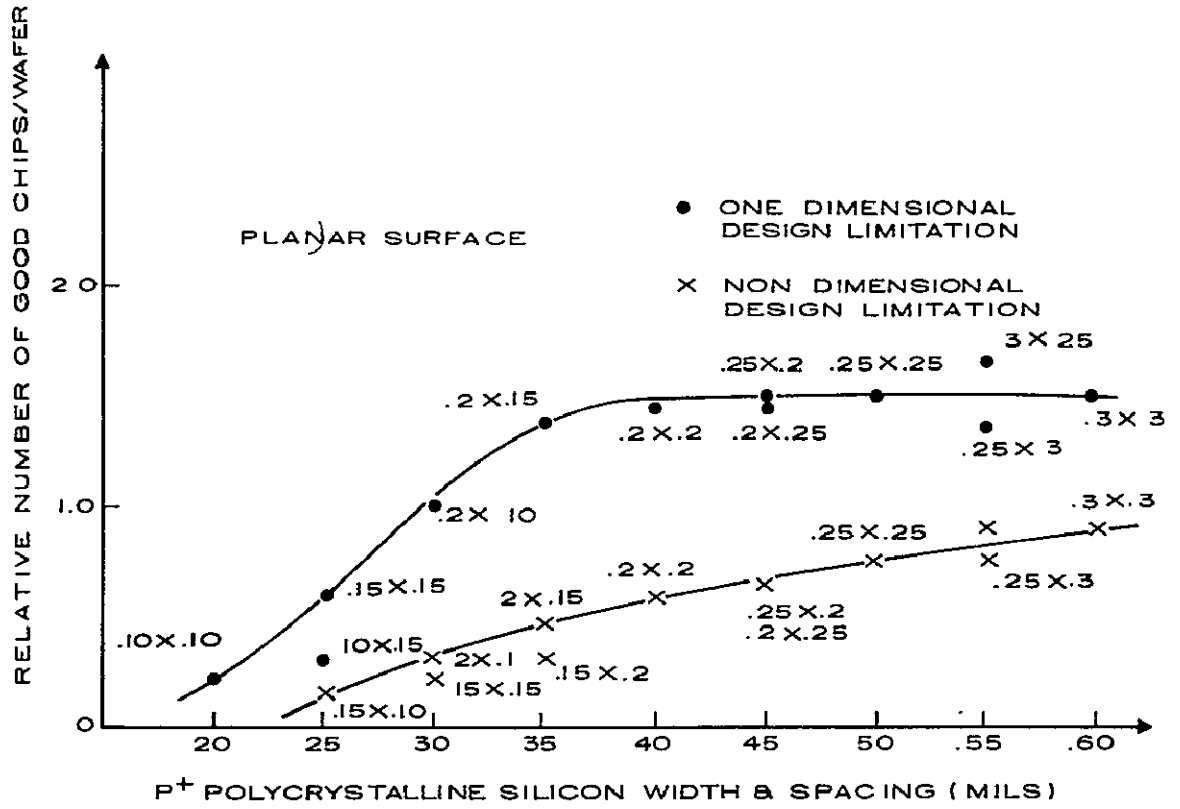

Figure 18. Good chips per wafer as a function of width and spacing, polycrystalline silicon.

Additional data must be generated for nonplanar polysilicon lines and spacings. Also, data will need to be generated for the case of N+ doped polysilicon layers since, in some applications, these are advantageous.

C. Contact Openings

In the area of contact openings, the data are too preliminary to generate an optimization curve. Applying Eq. (6) to the data in Fig. 12 indicates that for the two-dimensional case, the optimum contact size (square opening) appears to be between 0.15 x 0.15 and 0.20 x 0.20. The data yield essentially the same value for the relative number of good chips per wafer for contact sizes between 0.20 x 0.20 and

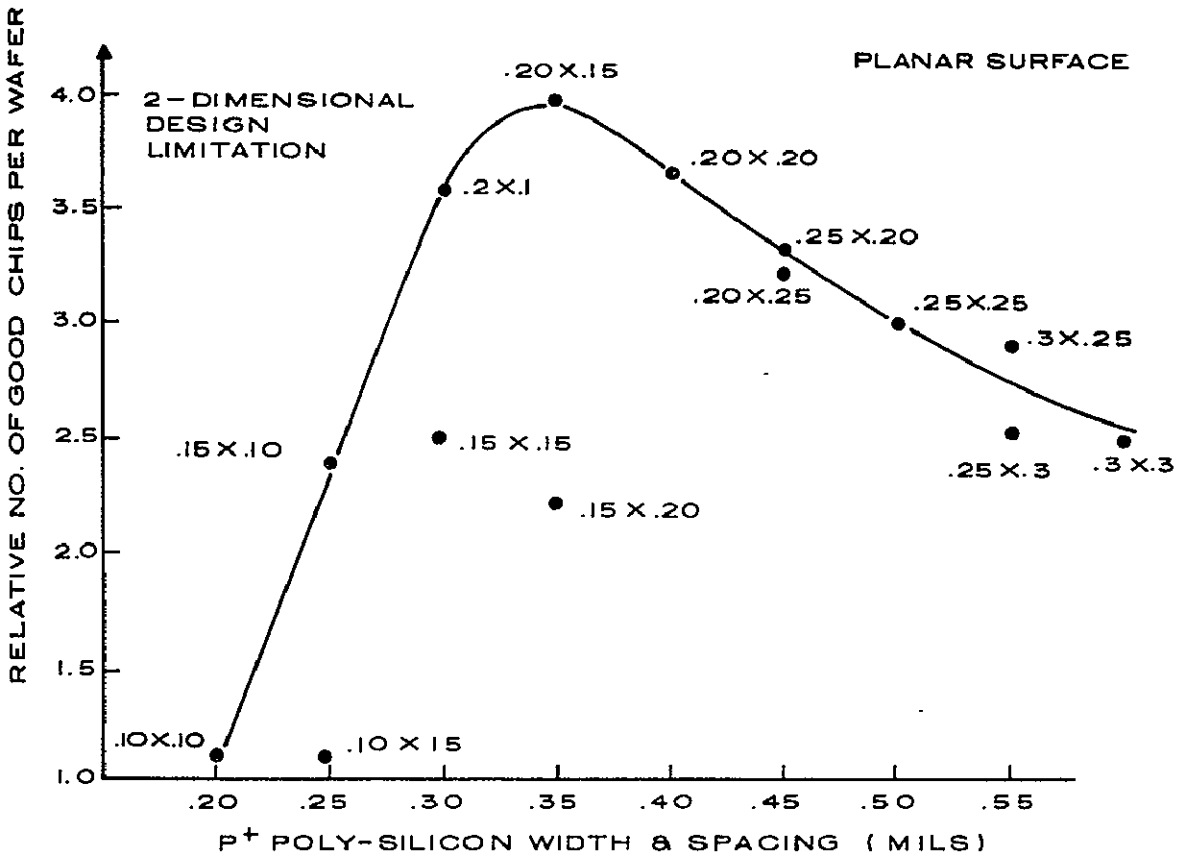

Figure 19. Good chips per wafer as a function of width and spacing, polycrystalline.

0.16 x 0.16 mils. For the one-dimensional case, the optimum size is greater than 0.20 x 0.20.

D. Metallization

Considering, first, the two-dimensional case [Eq.(6)], the results for optimizing aluminum on a planar surface are shown in Fig. 20. The results show a flat portion with a center value of 0.3 x 0.2 mil. It is felt, therefore, that this represents an optimum value, especially on planar surfaces. When compared with optimum epi-silicon or poly-silicon dimensions, it is seen that metal represents the single most

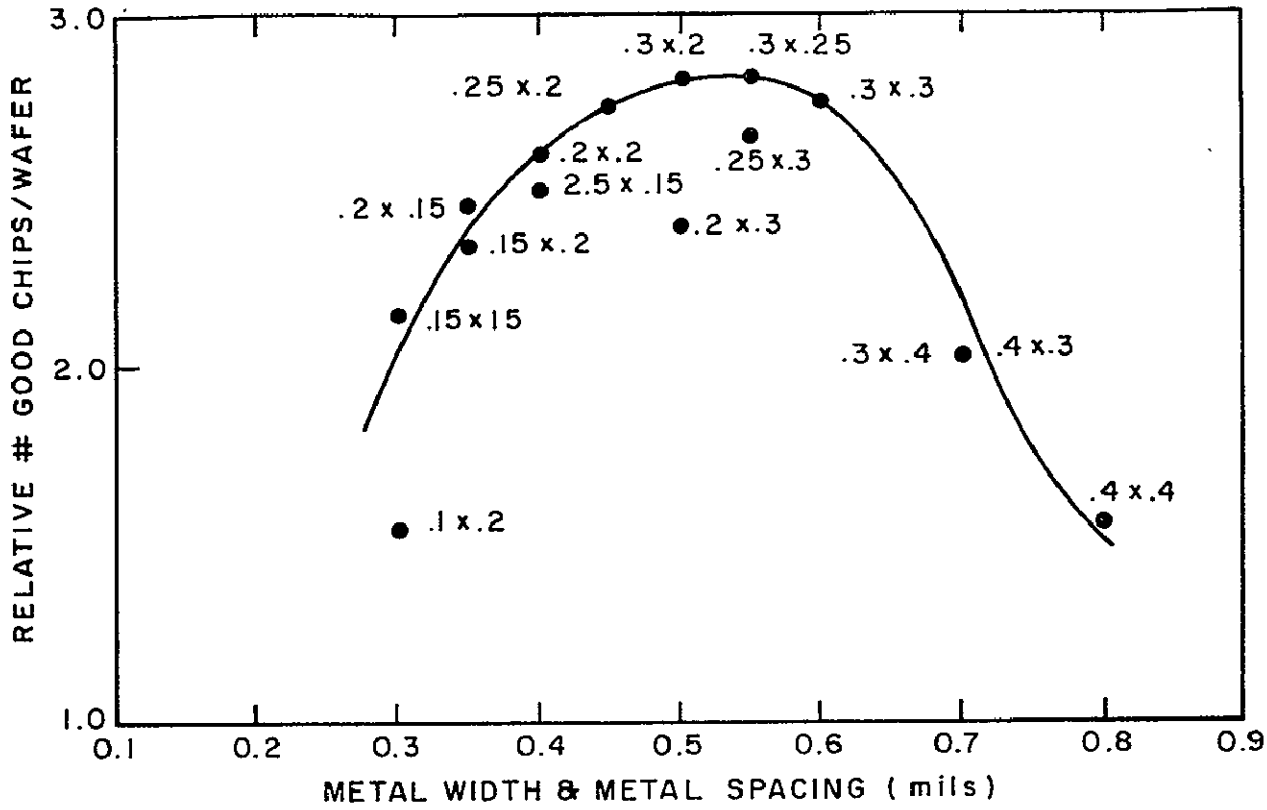

Figure 20. Good chips per wafer as a function of width spacing, planar surface, metal limited in both directions.

dominant element in SOS/MOS packing density. This is also true in other technologies as well, and shows the advantage of silicon-gate technology, especially that incorporating double layer polysilicon.

Using Figs. 13 and 14, a similar curve for nonplanar surfaces can be generated and a comparison of this relationship with that shown in Fig. 20 is given in Fig. 21. It is seen that the data show considerably less variation for nonplanar surfaces, and it would, therefore, be more difficult to determine an optimum value. It is felt, however, that the planar optimum value is a suitable estimate for the nonplanar value, and, hence, 0.3 x 0.2 mil is considered the optimum width and spacing for aluminum metallization.

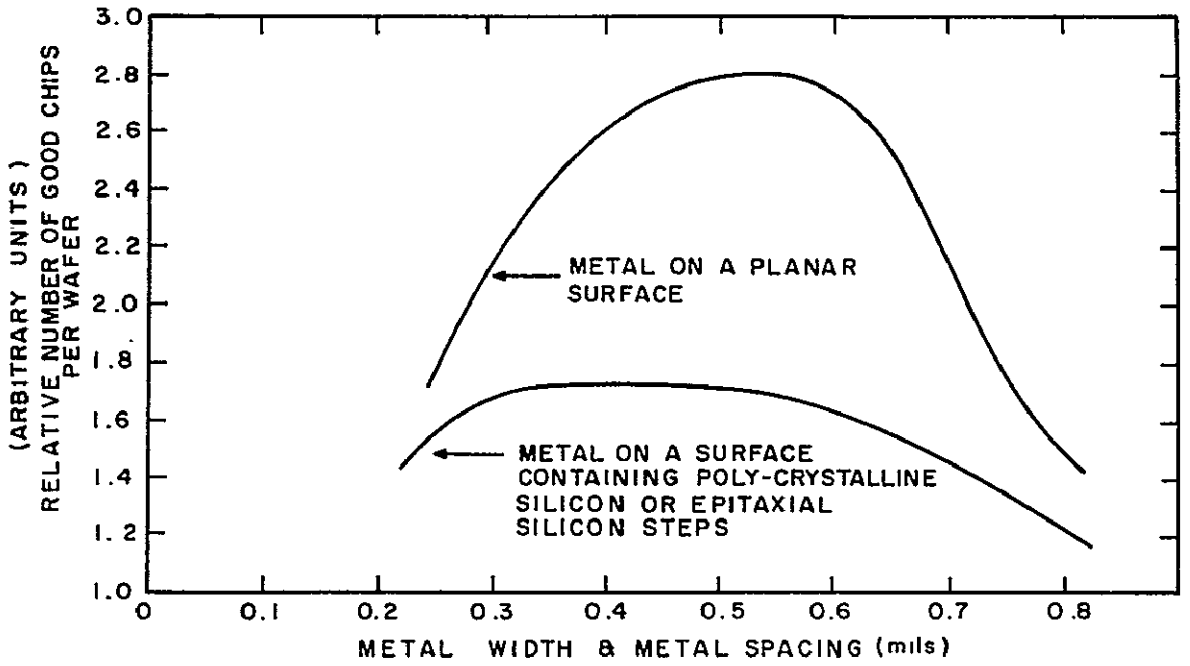

Figure 21. Good chips per wafer as a function of width and spacing, planar and nonplanar surfaces, metal limited in both directions.

Another significant result is the substantial reduction in the relative number of working chips per wafer which can be expected due to the nonplanarity of the surface. This is, of course, due to the lower yield values as given in Figs. 13 and 14. This points up the second technique, that of planar technology, which is being used in the industry to increase packing density through reduced dimensions. As can be seen from Fig. 21, it is possible to produce more working chips using 0.15 x 0.15 metal width and spacing on a planar surface than by using 0.3 x 0.2 mil dimensions on a nonplanar surface. In order to take advantage of this improvement in aluminum metallization, however, it is necessary to have an MOS planar metal gate process, and this has been done by several companies.

There are two contrasting viewpoints, therefore, concerning the direction that high density LSI will take in the future; one improves packing density by using more polycrystalline silicon layers with its improved yield characteristics and, in essence, builds vertically. The second relies on reducing dimensions significantly by having a planar surface. One can only speculate on which approach may dominate since the data presented here clearly demonstrate that both techniques will give improved packing density for a given yield figure.

Calculations have also been carried out for the one-dimensional case using the data in Figs. 13 and 14, and inserting them in Eq. (7). Figure 22 shows the results for the planar case, where it is seen that

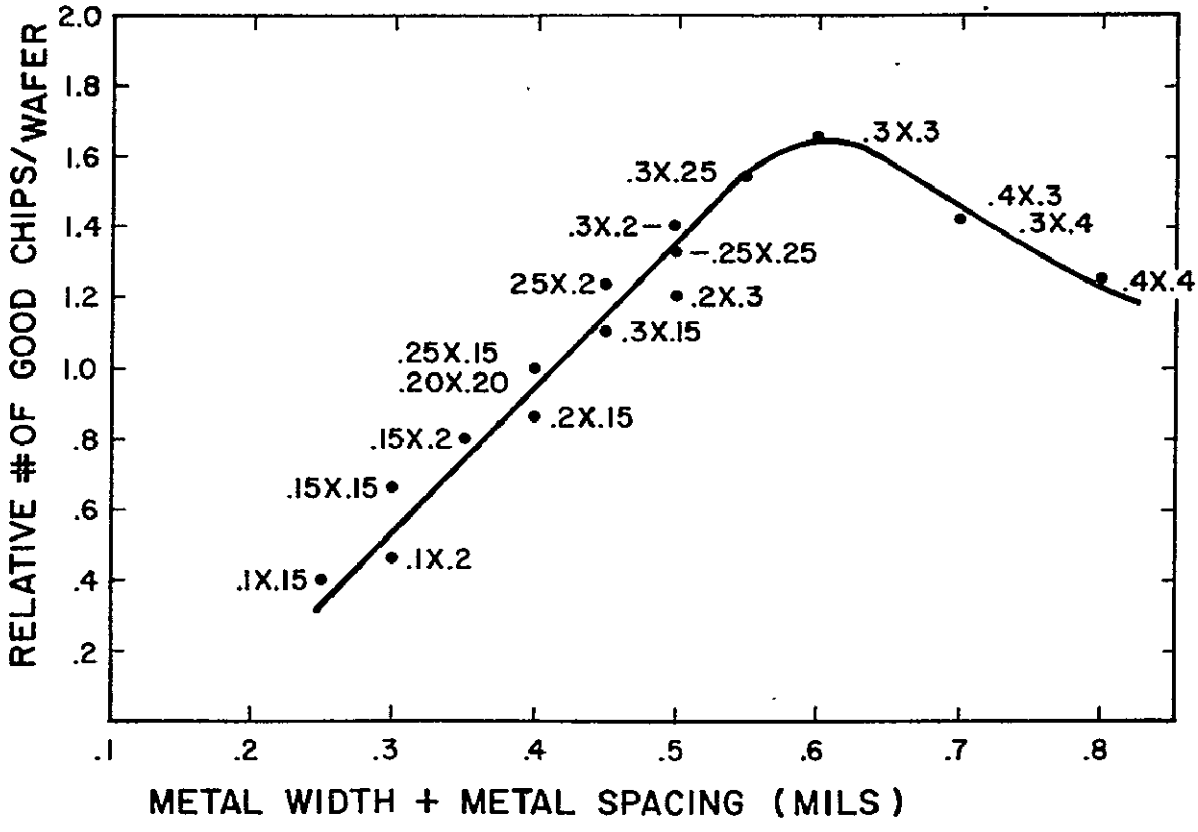

Figure 22. Good chips per wafer as a function of width and spacing, planar surface, metal limited in one direction.

the peak has shifted to 0.3 x 0.3 mil. This is to be expected since the reduction in chip area occurs more slowly with the metal width and spacing (linear) than for the two-dimensional case (quadratic) and hence, is not able to offset the resulting yield reduction at the tighter dimensions. A comparison with the nonplanar case is shown in Fig. 23. The optimum values are represented by a range of dimensions from 0.3 x 0.3 mil to 0.4 x 0.4 mil where, again, the number of good chips producible on a planar surface is substantially higher than for the nonplanar case.

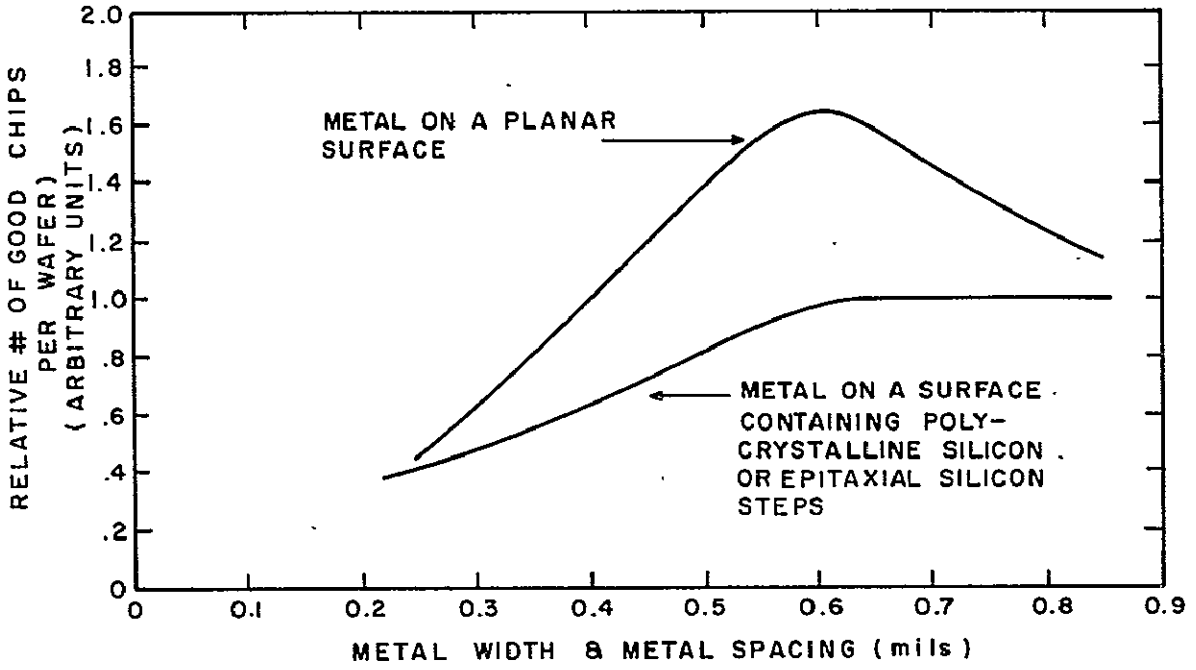

Figure 23. Good chips per wafer as a function of width and spacing, planar and nonplanar surface, metal limited in one direction.

For the condition where the number of good chips is only related to yield [Eq.(8)], the results are given in Fig. 24. This shows the advantage of using extremely loose dimensions when laying out areas of an array which are not metal-limited.

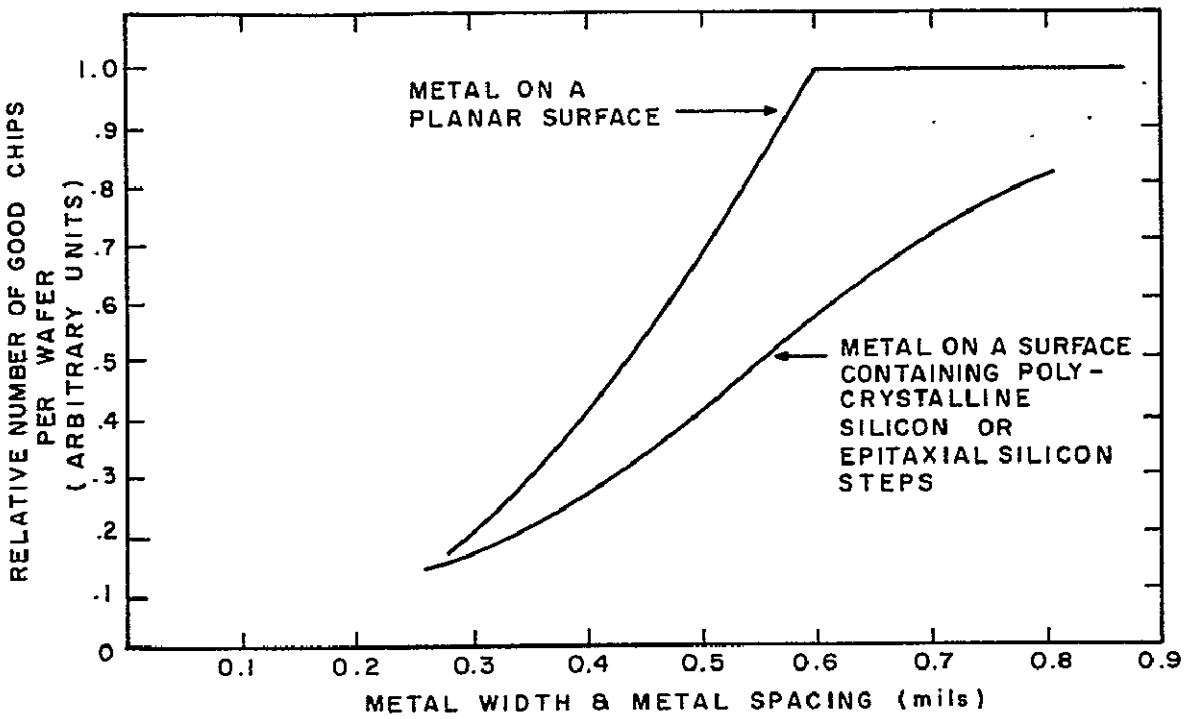

Figure 24. Same conditions as Fig. 23 with number of good chips only related to yield [Eq.(8)].

E. Summary

A set of design rules can, therefore, be generated using this mask set which are considered optimum for a particular technology. In the case of the silicon-gate deep-depletion CMOS/SOS process, the data indicate that the dimensions listed below are close to optimum values.

Definition	Dimension (mils)
Epi-silicon width	0.10
Epi-silicon to silicon spacing	0.10
Polysilicon width	0.20
Polysilicon to silicon spacing	0.15
Contact opening (square)	0.16 x 0.16 - 0.18 x 0.18
Metal width	0.30
Metal to metal spacing	0.20

It should be noted that the curves were generated using the combined values of level width plus level spacing. Since, in general, an array is limited by both the width and spacing, this is a legitimate combination. There are cases, however, where an array may only be limited by a width or spacing and the optimum value would, therefore, be slightly different.

It is also evident from the curves in this section that there are certain directions that process technology is likely to take in the future. The ability to define chemically vapor deposited (CVD) layers has been shown to be substantially better than that using evaporated films. In addition, it is possible to take advantage of the crystallographic nature of silicon to define extremely small patterns. Multiple CVD layers, therefore, seem to be a promising avenue for improving packing density. The results presented here clearly demonstrate the advantages of planar technologies as a substantially different direction toward increased packing density.

The last question worth addressing concerning the results in this section is whether the dimensions which were determined to be optimum represent a physical limitation on any of the process techniques used to obtain them. As described in Section II we are analyzing a process sequence comprised of:

(1) Thin film deposition or growth
(2) Photoresist techniques
(3) Etching techniques
(4) Doping techniques

It is felt that one or more of these techniques are limiting the minimum dimension associated with various layers. Photoresist appears to be the area of least limitation, especially with planar geometries. Concerning epitaxial silicon, film deposition appears to be the major limitation. For polysilicon, etching techniques seem to dominate as is the case for contact openings. Aluminum definition appears to be a

function of both the deposition system (or technique) and the etching technique.

In conclusion, the various test patterns described in Section II were used to generate process-dimension yield data which were transcribed into design curves showing optimum values for circuit layout. These curves also pointed to directions that future technologies may take in order to obtain increased packing density while maintaining present yield levels.

V. TECHNIQUES FOR YIELD IMPROVEMENT

The last two sections were concerned with characterizing a particular process and, in effect, establishing a baseline for yield values associated with particular process sequences. Once this has been done, the various test arrays can be used to analyze new process techniques in order to determine whether or not they result in improved yields for a given dimension. The following subsections will describe examples of this technique which will remain an ongoing study within RCA as long as new process innovations are being developed.

A. Polysilicon Gate Material

One simple yield-improving technique is found by comparing Fig. 17 with Fig. 19. By using the deposition and defining techniques of epi-silicon (Section II.A) in place of those used presently for polysilicon (Section III.B), substantially tighter dimensions can be used while maintaining high yield levels. It is felt that this is a result of both a change in the crystalline structure of the gate material on the sapphire (polycrystalline versus single crystal) and the thin oxide technique used to define it. The resulting material in the channel region of the devices is, of course, polycrystalline silicon and, hence, only gains from the defining technique. Long runs of gate material on sapphire, however, are common in many LSI arrays, and substantial yield improvements may be anticipated.

A second technique which is presently under investigation is the use of ion implantation to define the gate material. Since the pattern need only be defined in photoresist and is transferred to the gate material by boron implantation, it is felt that this technique will lead to substantial yield improvements in the area of gate material definition.

B. Contacts

There appears to be a rapid drop in yield when attempts are made to define contact openings less than 4.0 μm. Since the photoresist pattern appears well defined, this may be a fundamental limitation of the wet chemical technique. Therefore, techniques such as plasma etching and ion-beam milling need to be investigated.

C. Metallization

Experiments have been conducted which compared aluminum deposition in a Sloan electron-beam system with a filament system which deposited downward onto a two-dimensional wobbler. The results are shown in Fig. 25. Data were taken on two lots of wafers (five wafers per lot), and then the wafers were stripped of aluminum and remetallized in the opposite system. The corresponding measurements were consistent and showed the results given in Fig. 25. It is possible, therefore, to use these test patterns to make accurate equipment as well as process comparisons in order to determine the best (highest yield) approach.

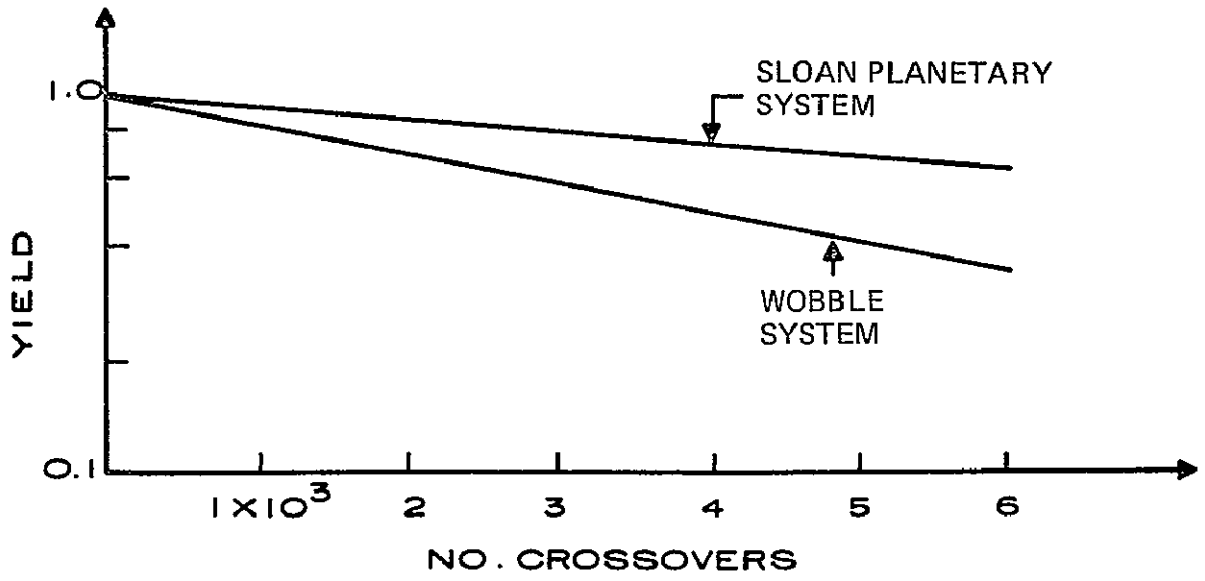

Figure 25. Metal continuity over polysilicon steps.

In the area of aluminum metallization a second comparison was recently completed. This was a comparison of wet chemical patterning of aluminum versus ion-beam milling. Ion-beam etching has been described in the literature (refs. 5,6) and, in general, its advantages are related to the nonchemical nature of the process. The results are shown in Fig. 26. The narrowest line mask was used (0.10 mil) and the metal thickness was reduced to 5000 Å. Using either Shipley 1350J or Waycoat 43, it was possible to define and mill the metal patterns. This was not possible previously due to the undercutting of the photoresist pattern during etching. A comparison with Fig. 13 shows that better yields resulted using Waycoat and chemical etching with thicker metal (14,000 Å), but it was now possible to define 0.10-mil lines with a nonzero yield curve.

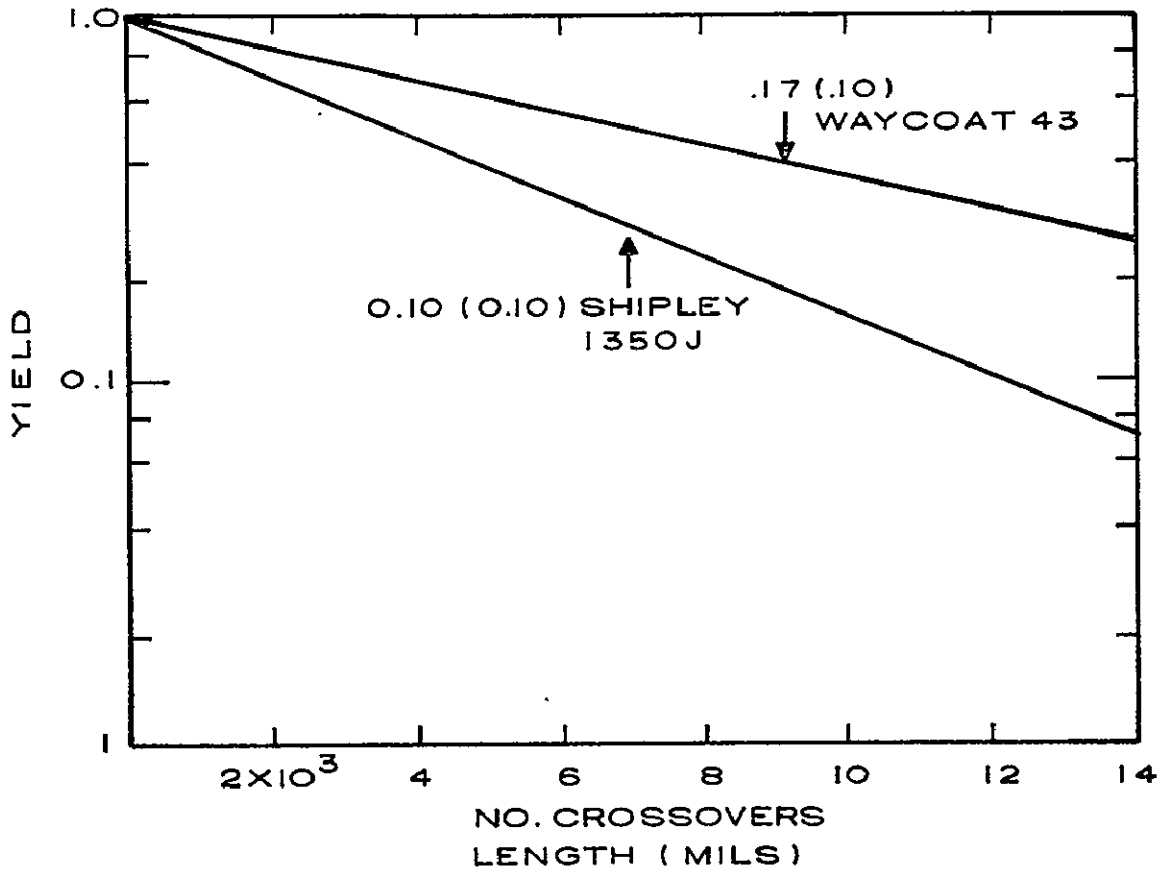

Figure 26. Metal continuity over epi-silicon steps.

The increased dimension, using Waycoat, was a direct result of an increase in photoresist width which was replicated exactly in the aluminum pattern. Additional experiments need to be carried out, of course, in order to ascertain the true usefulness of this technique, but it appears quite promising.

New techniques, therefore, are being investigated in various areas of SOS technology for the purpose of yield improvement through the application of special test patterns which are sensitive to the process-dimension interaction.

VI. ADDITIONAL APPLICATIONS

There are several applications of these test patterns and their resulting data which are being contemplated or are in the initial stages of development. Some of these applications will now be described.

A. Yield Prediction

Once sufficient data have been generated concerning the yield versus physical dimension for all the various parameters that comprise an LSI technology, it will be possible to predict the expected yield of an integrated circuit while it is still in the layout stage. It will only be necessary to know the physical dimensions of the various layers (lengths, widths, spacings, openings, etc.) in order to calculate the yield for that layout.

Assuming that both the layouts and the yield data exist in the same computer, various layouts can be analyzed from a yield maximization standpoint, automatically, by computer. In addition, a running yield tabulation can be made as various areas of the LSI array are digitized and stored. As the overall chip area becomes known, it will be possible to calculate chip cost since the yield, chip area, wafer area, and processing costs are known. This permits an input to marketing even before the circuit has been completely laid out and well before masks have been generated.

B. Process Reliability

Several specific areas of reliability can be addressed with these test arrays. It has been suggested that metal migration can be investigated as a function of such physical parameters as metal width, metal thickness, and surface typology. Using constant current sources, the current density can be increased monotonically until failure occurs, and then the "probability" of failure can be ascertained as a function of the various parameters.

Similar tests can be conducted concerning the channel oxide and field oxide reliability by measuring the dielectric strength as a function of various process parameters and physical dimensions. The gate-to-substrate or metal-to-substrate voltage can be increased until failure occurs, and again the probability of failure can be determined as a function of various parameters.

The experiments, as described above, can also be performed as a function of temperature. Bias-life failure mechanisms at elevated temperatures have been rather difficult to determine on actual integrated circuits. Problem areas such as metal neck-down over steps as well as channel oxide breakdown and field oxide failure have been suggested. All of these areas can be easily addressed using the suitable test patterns.

C. Diffusion Studies

Using the various test masks, some interesting impurity diffusion experiments can be carried out. The SPAR permits the investigation of the closeness of two adjacent diffusions. Mask levels 2A through 2E can be used to define diffused areas in either SOS films or bulk silicon substrates of the opposite conductivity type. Since these diffusions represent closely spaced, isolated diodes, they can be interrogated for diffusion short-circuits as a function of length, separation, and applied voltage. The separation can be thought of as the source-to-drain spacing of MOS devices, and the failure probability or yield data can be determined as a function of LSI array channel width.

Diffusion studies performed on bulk silicon substrates are more useful since diffusions are used as tunnels and also for device isolation. The PAS mask levels 4A through 4F can be used to analyze the continuity of diffused lines as a function of length and width. In addition, the diffused region represents a diode of variable length and width whose properties can be investigated. Various bulk surface passivation techniques can be studied using the SPAR, since the area

between the diffused regions, if inverted, will become conductive. New passivation techniques such as ion-implanted surfaces or SIPOS (ref. 7) must be analyzed from an LSI standpoint (i.e., is the passivation successful over several inches of length?).

Using PAS mask levels 4A through 4F, double-diffused structures can also be fabricated. As an example, 4A can be used to obtain a "well" diffusion while 4C can define a second diffusion within the well region. Measurements between the second diffusion and the substrate permit evaluation of the well integrity. The probability of a localized diffusion failure causing source-drain-to-substrate short-circuits can be determined as a function of well and source-drain area.

D. Yield Modeling

Yield modeling is the application of experimentally determined yield data to various defect density distributions which "may" be the underlying cause for the yield reduction with a particular parameter (area, length, number of crossovers, etc). The initial model as proposed by Hofstein and Heiman (ref. 8), coincidentally for SOS/MOS devices, assumed a totally random distribution of defects which results in the expression for yield (Y):

$$Y = e^{-AD} \tag{9}$$

where A is the area of the integrated circuit and D is the average number of effective defects. Experimentally determined yield versus area curves, however, have shown that, for LSI arrays, Eq. (9) can be overly pessimistic, as was shown by Moore (ref. 9). This led to several papers dealing with nonrandom defect distributions. Warner (ref. 10) characterized the yield as the "sum" of individual terms, each of which represented a discrete area of a wafer over which the defects were randomly distributed. Equation (9), therefore, became:

$$Y = Y_o + Y_1 + Y_2 \ldots$$

or

$$Y = A_o e^{D_o A} + A_1 e^{-D_1 A} \ldots$$

where: $A_o + A_1 + A_2 \ldots = 1$

The A_n terms represented the area over which the average defect density equaled D_n. Assuming infinitely small areas,

$$Y = \frac{1}{\alpha} \int_0^{\alpha} e^{-AD(a)} \, d(a) \tag{10}$$

where α represents the total area of the wafer and D(a) the average defect density over the incremental area d(a). Expressing Eq. (10) in polar coordinates

$$Y = \frac{1}{\pi R^2} \int_0^{2\pi} \int_0^{R} e^{-AD(r\theta)} \, r dr d\theta \tag{11}$$

A defect density distribution which increases radially has also been discussed in the literature (ref. 11). Assuming no theta (θ) dependence, Eq. (11) becomes:

$$Y = \frac{2}{R^2} \int_0^{R} r e^{-AD(r)} \, dr$$

As an example, consider a wafer having three different average defect densities as a function of radius. Then:

$$Y = \frac{2}{R^2} \left[\int_0^{R_1} e^{-AD_1} \, r dr + \int_{R_1}^{R_2} e^{-AD_2} \, r dr + \int_{R_2}^{R} e^{-AD_3} \, r dr \right.$$

integrating:

$$Y = \frac{R_1^2}{R^2} e^{-AD_1} + \frac{R_2^2 - R_1^2}{R^2} e^{-AD_2} + \frac{R^2 - R_2^2}{R^2} e^{-AD_3} \qquad (12)$$

letting

$$A(R_1) = A(R_3) \text{ and}$$

$$2A(R_1) = A(R_2)$$

Equation (12) becomes

$$Y = \frac{e^{-AD_1}}{4} + \frac{e^{-AD_1}}{2} + \frac{e^{-AD_3}}{4}$$

if we further let

$$2D_1 = D_2 \text{ and}$$

$$3D_1 = D_3$$

we have

$$Y = \frac{e^{-AD_1}}{4} + \frac{e^{-2AD_1}}{2} + \frac{e^{-3AD_1}}{4} \qquad (13)$$

This expression is plotted in Fig. 27 for the two cases where:

$$\frac{D_1 + D_2 + D_3}{3} = 70 \text{ defects in.}^2$$

and

$$\frac{D_1 + D_2 + D_3}{3} = 42 \text{ defects in.}^2$$

Also shown in the figure are the totally randomly distributed cases

$$Y = e^{-70A}$$

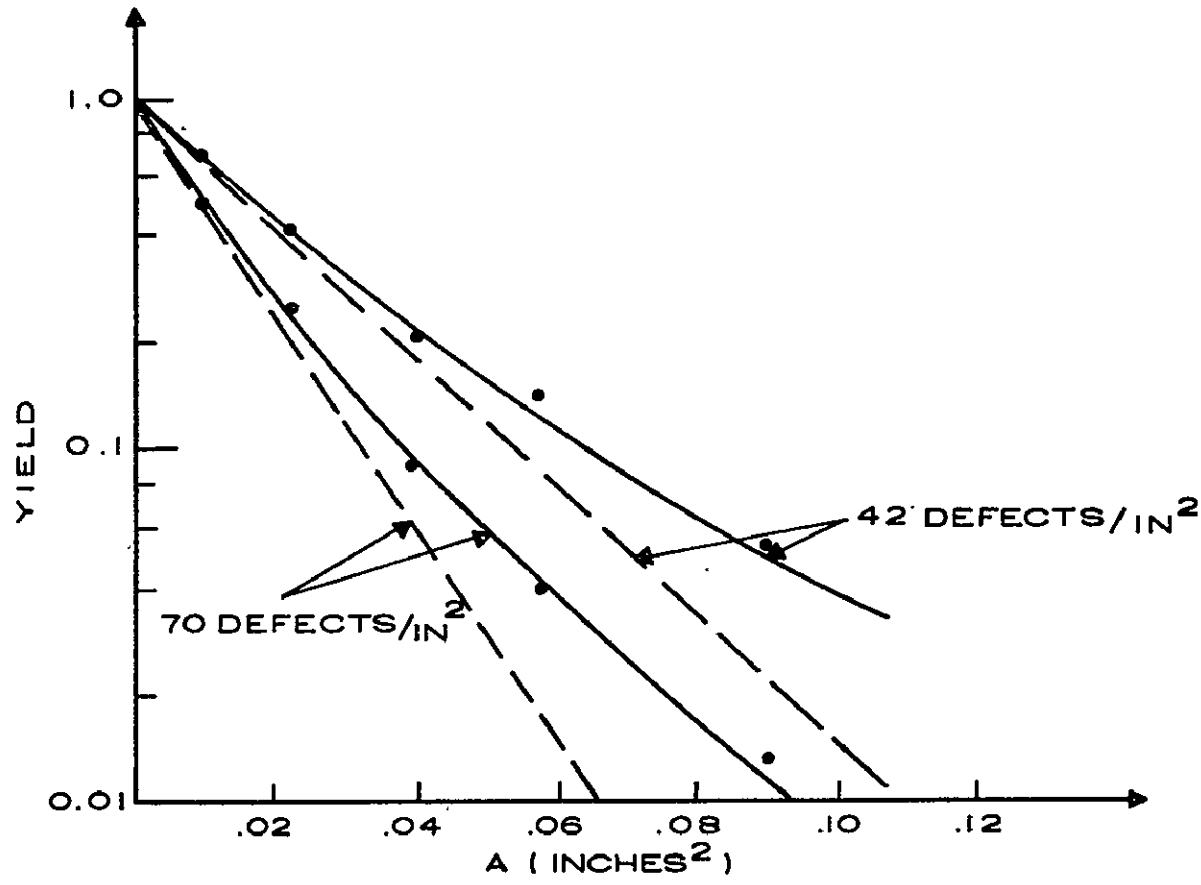

Figure 27. Yield modeling.

and

$$Y = e^{-42A}$$

A computer program was written by N. Goldsmith to verify Eq. (12). Defects were distributed over a wafer having a weighted probability with radius as shown in Fig. 28. Yield data were compiled as a function of circuit area, and the average yield was determined by generating repeated defect distributions and averaging the resulting yield values for each circuit area. The yield values generated by this program are shown in Fig. 27 where it is seen that they are in good agreement with Eq. (12).

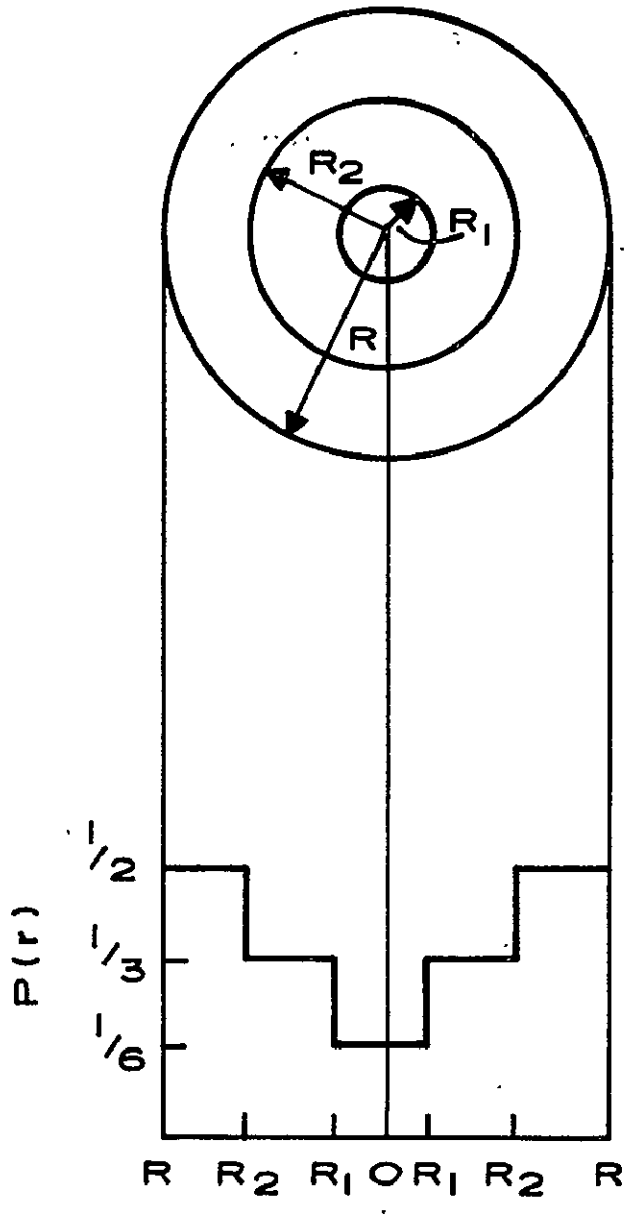

Figure 28. Wafer with weighted probability with radius.

The yield data described in Section III show a simple exponential [Eq.(9)] dependence; therefore, it is not yet necessary to resort to composite models to explain the present results. It should be noted, however, that there may also be yield-limiting mechanisms which are associated with the registration or alignment of one mask level with

another. Such problems as mask run-out or rotational misalignments will cause a radial error distribution and an "apparent" radial defect density. This is especially true of arrays with excessively tight alignment tolerances where even thermal differences from alignment to alignment can be sufficient to cause radial errors. It will be necessary to generate additional data, however, before attempting any extensive defect analysis.

VII. CONCLUSIONS

It was the object of this program to develop a method for determining the applicability of a particular process for the fabrication of large scale integrated circuits. To this end, test arrays were designed, built, and tested. It has been shown that by applying them to a particular process, the arrays achieve the desired results. In this case, the process under analysis was the silicon-gate deep-depletion CMOS/SOS technology and the test arrays have characterized it from the realm of process-dimension interrelation as well as the process-sequence-to-process-sequence interrelationship. The strong points of the present process, such as epi-silicon definition, as well as the weak points (channel dielectric) have been exposed for analysis.

From the application of the test arrays it was possible to generate a set of optimum dimensions which would maximize the process output and correspondingly minimize cost in the fabrication of LSI arrays.

Since the initial incorporation of the test arrays into the process characterization study, several additional applications of the patterns became apparent. The arrays have been used in a comprehensive program to achieve improved yields through the introduction of new equipment and techniques. Among these are such areas as ion implantation and ion-beam etching. The arrays have demonstrated the advantages of such process innovations as multilevel polysilicon and isoplanar technology and raised the question, "What direction will future technologies take?"

Several new applications of these test arrays are being contemplated and are outlined herein. These include such areas as yield prediction, yield modeling, diffusion studies, and process reliability. There is little doubt that the PAS, SPAR, and CAR will find additional applications both within and without the realm of SOS and that these applications will lead to improved yields, higher packing densities, and more complex LSI arrays.

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